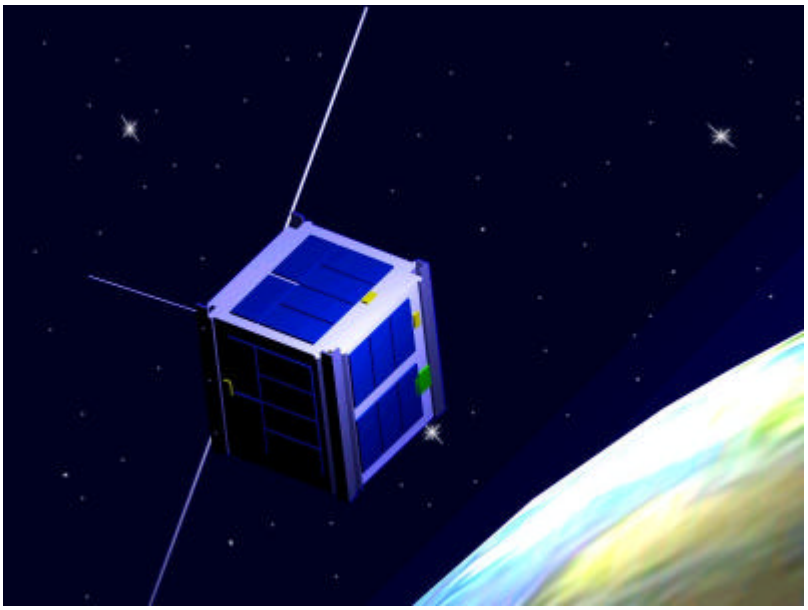
Special Course at Eltek, DTU:

Design of a DC/DC converter for DTUsat



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Abstract

This paper is a continuation of our project “Design of a Power Supply System for DTUsat”. Where the first paper was about the design of the entire power supply this project is mainly about the design of the DC/DC converter. Also the electrical design of the housekeeping systems etc. is described in detail in the paper. Finally some battery tests are described and the results analyzed. This includes temperature tests, and low pressure tests.

Contents

Appendices

1. Introduction

This project is a continuation of our system design of the powersupply for the DTUsat student satellite. This project mainly deals with the electrical design of the powersupply unit. Also we follow up on the unsolved problems discovered during the first project. These are:

- Purchase of solar cells
- Purchase of Li-Ion cells that are packed in a cylindrical package
- Vacuum test of the cylindrical cell, and of the pouch packaged cell
- Temperature tests of the cell we're going to use
- Thermal calculations for verification of the battery operation area
- Determination of the maximum allowable noise on the output
- Thermal calculations for power components on PSU
- Design and layout of the entire PSU.
- Optimization of the overall efficiency

In the last paper we also stated that the final components must be exposed to a total dose radiation test in order to determine the long term changes. By evaluating the data from the previous test performed in December 2001 it has been decided to cancel any further tests. This is due to the fact that all components came out with only slightly changed characteristics even at 10 krad. Also, further investigation in the NASA publications reveals that the poorest COTS component worked until about 15 krad. These numbers are far above the expected dose of less than 2 krad for our configuration (orbit and mechanical design) per year.

One additional to-do item was a latch-up test of the electronics of the entire satellite. Currently we expect to perform this test sometime in the end of September 2002. We therefore can't discuss that issue in this paper.

Finally we suggested a simulation with a satellite model that had body mounted solar cells in order to simulate the satellite in orbit. Since we are nowhere near a complete satellite at the present time this item has been postponed too.

2. Changes in Specifications from Previous Project

The mechanical design of the satellite has progressed a lot. This has resulted in some changes of the design specifications, most importantly the size of the PCB, which is now:

- The physical size of the PCB (printed circuit board) is 8 x 6 cm^2
- The size available for components on the PCB is 7,5 x 5 cm^2
  Note: the connector is located outside of this area

Actually the available area will be somewhat lower because we need some space for mounting. The exact location and design of these has not yet been determined.

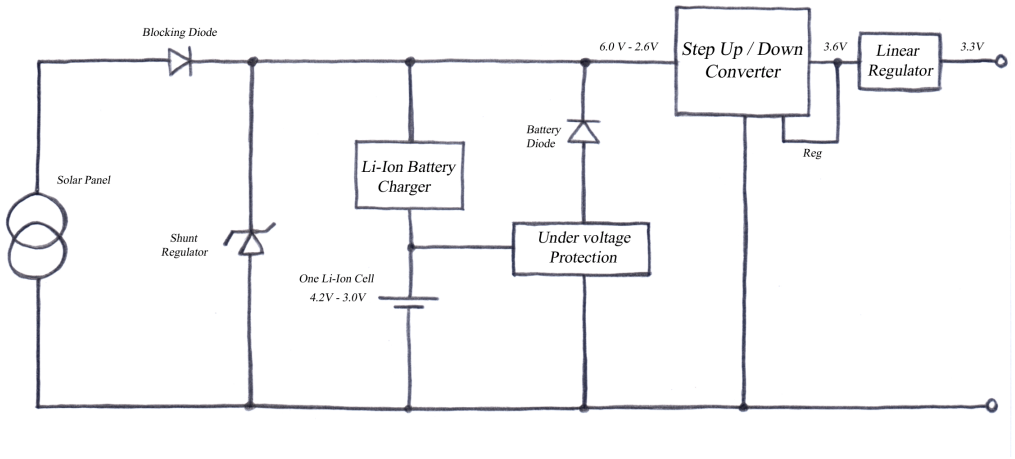
Also the power and weight budgets have been changed slightly. The changes are, however minor, and will not be discussed here. The power budget can be seen in Appendix A, and the weight budget in Appendix B.

3. Electrical Power System Architecture

To provide a stable dc-bus voltage of 3.3V there are two possible solutions, one that requires one battery and another that requires two. The two topologies have both advantages and disadvantages so there will be a tradeoff between the two solutions. Notice that none of the house keeping data measurements are shown on the following figures.

3.1 Using one Li-Ion Cell

The electronic structure is shown as a block diagram in the figure below:



The blocking diodes prevent the solar panels from discharging through each other and the shunt regulator prevents the solar panel voltage from exceeding a value that can destroy the devices attached to the unregulated bus.

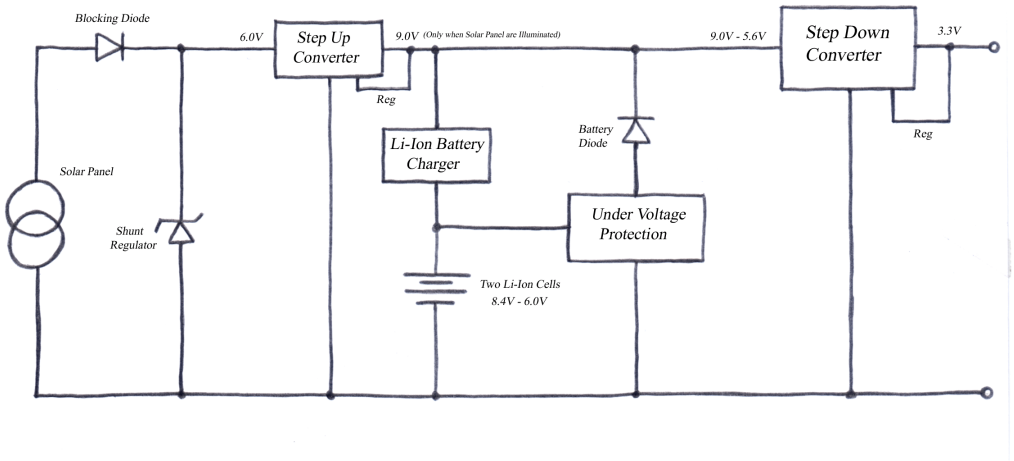
The Li-Ion battery is protected against overcharging by the charging circuit. When the solar panels are illuminated the battery diode is reversed biased. This diode will ensure that the battery is only charged through the charging circuit. During eclipse the voltage from the solar panels is zero and the battery diode will be forward biased, thus allowing the battery to discharge through the undervoltage protection circuit. This circuit prevent the battery from being over discharged by cutting off the battery when the voltage reaches 3,0 V.

Because the unregulated bus will be about 6 V when the solar panels are illuminated and between 4.2V to 3.0V minus a diode voltage drop, the dc-dc converter has to perform both step up and step down to provide a stable dc-bus voltage of 3.3V. Unfortunately a converter that can do this has a great deal of AC ripple on the output. Therefore the linear regulator has been added to remove that AC ripple. The linear regulator has a voltage drop of about 0.3V so the output from the DC-DC converter has to be about 3.6V in order to provide the 3.3V regulated dc-bus.

It may be better to have a linear regulator for every user on the regulated bus instead of only one, so that the total current of 1A does not have to be drawn through one linear regulator. If only one regulator is used it has to dissipate roughly $P_{max} = 1A \cdot 0.3V = 300mW$. This will most likely cause the regulator to malfunction because it can't dissipate the heat (some devices have internal temperature protection, so that the device may not be damaged permanently). By using more regulators it will ease the dissipation of heat and the noise that the different users send back will be reduced too.

3.2 Using two Li-Ion Cells

The overall structure is very similar to the one battery solution, so only the differences will be described.



To charge two series connected Li-Ion batteries requires at least 9 V, and the Li-Ion charger has to control the individual battery cell voltages to prevent overcharging because even though the total voltage of the series connected batteries is lower than 8.4V the voltage of one of the cells can exceed 4.2V and therefore become overcharged. This makes the charging circuit more complex than the single cell charger, but if a single chip solution is chosen the designer won't se much difference.

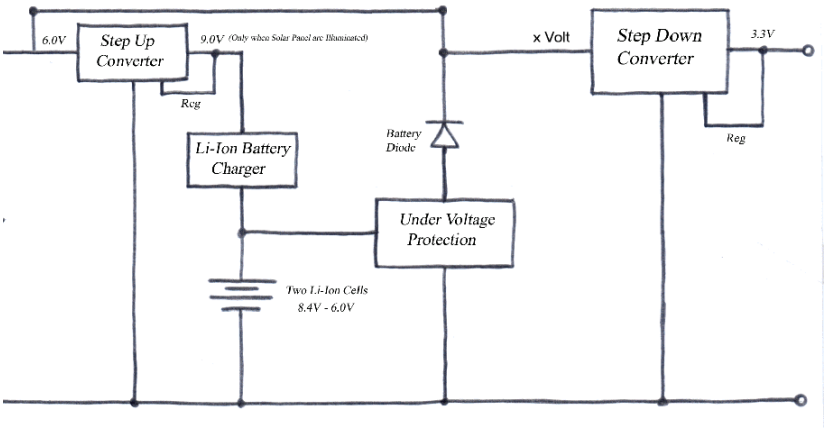
When discharging the two series connected cells a similar problem can arise: one of the cells can be over discharged even though the total voltage is not below 6,0V. Hence a more complex undervoltage protection circuit is needed. If a single chip solution is used there won't be much difference, but if the circuit has to be designed to be latch up free it will be more complex.

To provide the 9V that is required to charge the batteries a step up converter is needed because the solar panels will only provide about 6V. The unregulated bus voltage will be 9V while the solar panels are illuminated and while not the voltage is between 8.4 to 6.0V minus the diode voltage drop. The unregulated bus voltage will always be larger than the regulated one so a step down converter can be used. This type of converter does not have the same large AC ripples on the output as the step up/down converter so here the linear regulator is not needed.

This setup is more efficient than the one mentioned in section 3.1. Unfortunately the system engineering group has decided that the solution based on a single battery is going to be used. This is mainly due to the extra mass a second battery would require - and the difficulties in purchasing another battery. (Two batteries with half the capacity will only be slightly heavier, but it is difficult, if not impossible, to find them).

Notice that both solutions are missing a global latch up protection. Also some sort of current limiting circuit is missing, this is needed to prevent the solar panel voltage from decreasing if the rest of the satellite tries to draw too much power.

One might think that the step-up converter is only needed for the battery charger, and that you don't have to step-up the voltage delivered directly from the solar panels to the step-down converter, as shown in the figure on the next page.



This method doesn't work, however. The problem is that when the satellite is illuminated the voltage at node x should be 6,0 V, but the battery voltage is higher (up to 8,0 V), meaning that all power is provided by the battery. In the above figure the current is also allowed to flow from the battery back to the charger - this could be fixed by a diode (meaning further power loss), but this doesn't change the original problem. Some kind of switch could solve the problem, but at the cost of higher complexity.

4. Solar Cells

As stated in the previous paper we were going to purchase some second class cells from Spectrolabs. In the end it turned out that the cells that we needed wasn't on stock, and it is unlikely that they will become available again in the near future.

The Danish satellite Rømer is currently in the process of finding solar cells too. We have therefore joined them in order to get a better price on the cells due to a higher volume. We have been in contact with Emcore, they can currently deliver 4 x 3 cm^2 cells with an efficiency of 27%. The price for a bare-cell is USD 195. Including coverglass and interconnectors (CICed) the price is USD 240.

The size of these cells only allows 4 cells per side. This results in a voltage/current output of either 4,56 V, 860 mA or 9,12 V, 430 mA per side (either 2 or 4 cells in series). Neither of these configurations are desirable. The first requires a step-up converter in order to be able to charge the batteries, and the latter results in a high unregulated bus voltage (the regulated and unregulated busses are poorly matched). One benefit of the higher voltage is, that loss in the blocking diodes will be halved from $\frac{0{,}4\text{V}}{4{,}5\text{V}} = 8{,}9\%$ to $\frac{0{,}4\text{V}}{9{,}0\text{V}} = 4{,}4\%$.

We would therefore prefer to use 2 x 4 cm^2 cells. Emcore previously produced cells of this size with an efficiency of 26%. They are currently investigating whether they can supply us with cells of this size, and at what price.

It has been discussed whether it is necessary to use coverglass on the solar cells. Due to the low orbit (expected altitude of 650 km), and the short lifetime of the satellite (less than one year), it is not expected to be a necessity. Of course the cells for the Rømer satellite is going to be equipped with coverglass and if we're going to use the same cell size we're going to use coverglass as well.

Finally Emcore has informed that the coverglass is 500 µm thick, and the cell is 140 µm thick. This implies that the cells without coverglass are bendable. This is a nice property because it will ease the assembly of the cells on the body of the satellite.

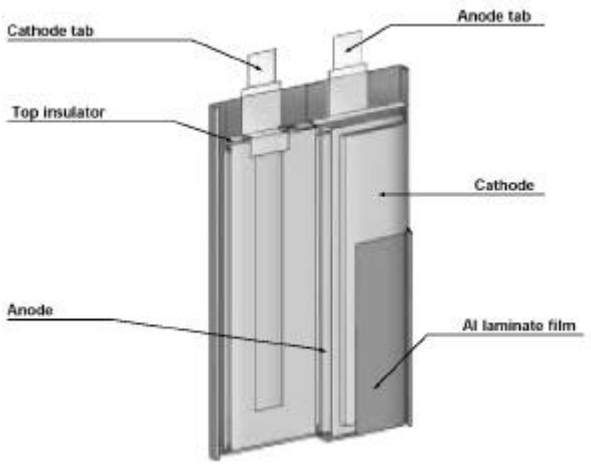
5. Battery

5.1 Battery Packagings

In the last report we found that the best suited battery chemistry for the DTUsat was a Li-Ion based battery. This means that there are two types to chose among, the Li-Ion polymer and the Li-Ion battery, where the last type is packed either in a cylindrical or prismatic packaging. They all have almost the same electrical and temperature characteristics. The physical construction that contain the battery has to be chosen with care, the container has to be able to withstand the rough demands required in space. In the following the three types of packaging will be described.

5.1.1 Aluminum Laminate Packaging

The Li-Ion Polymer battery is almost always contained in an Aluminum laminate film that only provides a soft shell around the battery, see the figure below.

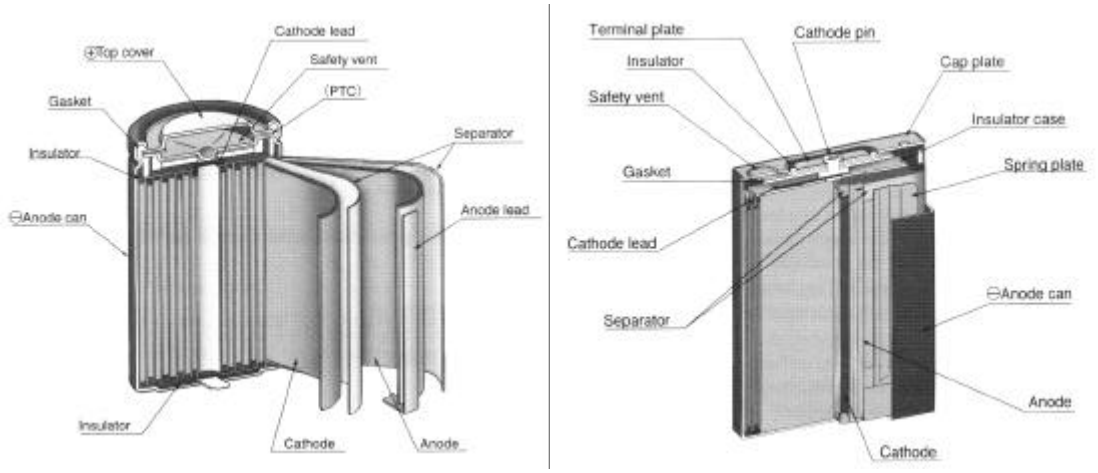


The cell is packed at low pressure but when the cell is brought into space where the pressure is even lower the cell will swell because of the few air molecules that are inside the foil packaging. If the molecules are inside the battery and not just between the outer Al laminate film and the battery, the swelling will cause the battery to loose capacity. Only tests can determine if the polymer battery can be used for space applications.

We have previously performed a visual vacuum test at a pressure of 0.085 Torr ($1 \cdot 10^{-4}$ atm) where the battery swelled to about twice the original thickness. We have later made a charge/discharge test at the same pressure that showed that the electrical characteristics were changed too. The test is described in section 5.3.

5.1.2 Cylindrical and Prismatic Packagings

The Li-Ion type cell is packed either in a cylindrical or prismatic structure, see the following two figures.



Both containers are made of metal and provide a constant pressure inside the battery even when they are brought into vacuum. So by choosing one of these there will be no vacuum problems.

These metal containers have a one-time safety vent that is activated if the internal pressure exceeds a specified value. Actually the safety vent is just a weakness of one end of the packaging that will cause it to break when the pressure inside the battery becomes too high - this is to avoid an explosion of the battery. This is in order to prevent that humans get hurt if they are close to the battery when, for some reason lots of gas is released inside the battery, usually due to a defective charging circuit.

For our purpose the safety vent has to be strong enough to withstand the vacuum. For the DTUsat a cylindrical cell will be used mainly because it was the only cell that could be achieved, but it is expected that a cylindrical structure is better to withstand vacuum than is a prismatic structure. One advantage of prismatic cells is that they are easier to mount inside the satellite.

5.2 Test of Li-Ion Battery Chargers

It was fairly early in the process decided that we wouldn't use a switch-mode based battery charger. The efficiency of this method is high, but it comes at a cost of a high complexity of the circuit. The major drawback of this is the PCB area required. Also the additional components consumes additional weight from a budget that is already tight.

The switch mode charger is opposed by the linear charger which features a high integration, and a small number of external components, usually a P-MOS transistor and some capacitors, but some chargers come with a build-in P-MOS. This might become a problem due to heat dissipation in vacuum. The ADP3820 from Analog Devices and BQ24200 from Texas Instruments are two different linear chargers that we have tested. The latter comes with a build-in P-MOS transistor.

Yet another kind of charger is based on pulse charging. Compared to linear chargers this should reduce the loss when charging the battery. The Maxim max1879 is an example of such a charger. It only requires one external P-MOS transistor and some capacitors and resistors.

We have tested a Li-Ion cell and a Li-Ion Polymer cell using each of the above mentioned chargers. The measurement is based on the ISA Data Acquisition Card we described in our last paper. To this a number (3) max144 12-bit 2 channel a/d converters have been connected. One ADC is connected to the input voltage and the battery voltage. The second is measuring the

temperature using an LM19 temperature sensor (used for a freezer test, see section 5.4), and the last ADC is connected to two max472 bi-directional current amplifiers, that measures the input current to the charging system, and the battery charge/discharge current. The measurements have been done every 10 seconds. This allows us to calculate the capacity of the cell as:

$C = \int_t U \cdot I \, dt$ [Wh]. Also we can measure the efficiency of the different battery chargers.

All tests have been made at room temperature. A plot of each test can be seen in Appendix C.1 and C.2. The chargers were set to limit the current to 500 mA, and the charging period would stop when the charging current was lowered to 50 mA. The discharge current was set by a resistor to approximately 500 mA, and discharge is terminated when the battery voltage reaches 3.0 V. A summary of the tests can be seen here:

Panasonic CGR18650H, Li-Ion cell (1500 mAh)

Charger	Filename	Battery capacity	Battery Input power	Battery efficiency	Charger efficiency
ADP3820	data.ny5	5581 mWh	6042 mWh	92,4%	not measured
BQ24200	data.ny4	5581 mWh	6082 mWh	91,8%	not measured
MAX1879	data.ny6	5664 mWh	6055 mWh	93,5%	not measured

Li-Ion Polymer cell (1000 mAh)

Charger	Filename	Battery capacity	Battery Input power	Battery efficiency	Input power	Charger efficiency
ADP3820	data.b1	3502 mWh	3838 mWh	91,2%	5053 mWh	76,0%
BQ24200	data.b2	3516 mWh	3820 mWh	92,0%	5163 mWh	74,0%
MAX1879	data.b3	3582 mWh	3887 mWh	92,2%	5190 mWh	74,9%

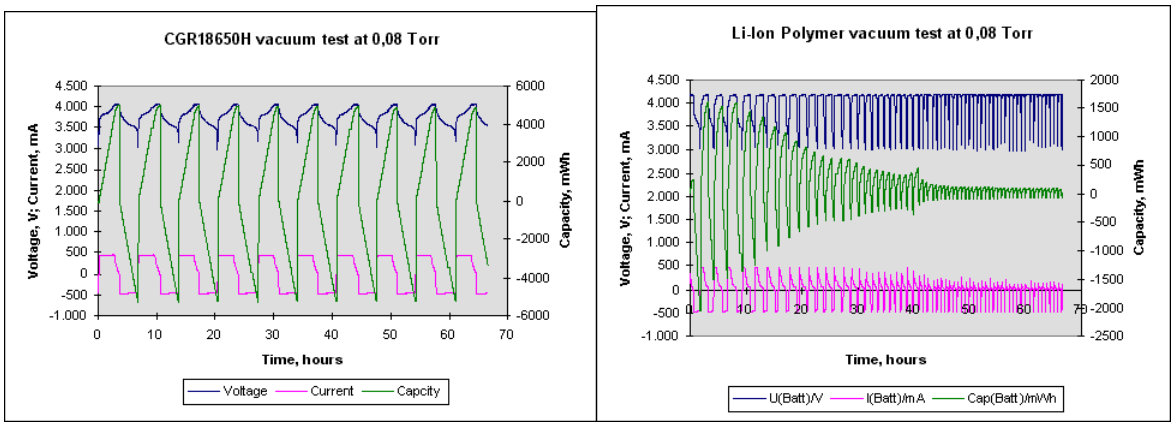
For the above tests the input voltage was 5V. If the input voltage was higher the MAX1879 charger would probably show about the same efficiency, while the other (linear) chargers would show a lower efficiency. For now we have decided to use the max1879 battery charger.

5.3 Vacuum Tests of Batteries

Even though other Cubesat satellites are using Panasonic cells similar to CGR18650H they don't provide any data regarding their usage in vacuum. We therefore decided to test both cells under vacuum conditions.

The results can be seen in Appendix C.3. Unfortunately the powersupply was not set correctly during the test of the CGR18650H cell, resulting in wrong current, and voltage measurements. These could be scaled to fix the mistake, but since it is of no significance we haven't done that. The test of the CGR18650H cell shows that the capacity is unchanged during the 66 hour (2 days, 18 hours) test.

The Li-Ion Polymer cell showed some rather different properties during the vacuum test. As seen on the figure in Appendix C.3, the capacity of the first cycle is only about 2000 mWh, compared to more than 3500 mWh at sea level. But even though the capacity is low to begin with, it is reduced further during the first 45 hours, after which it seems to somewhat stabilize at about 70 mWh.



The result of this test is that the Li-Ion Polymer packaging, as expected, wasn't sufficient for low pressure operation. This is due to the fact that the air molecules that are contained in the sandwich construction of the cell are allowed to expand, removing the layers of the cell from each other. This causes in effect the loss in capacity.

It has been suggested that one could take two PCBs and fix them on the two sides of the cell in order to avoid the battery to expand. We are in much doubt whether this method is sufficient. But since we are going to use other cells for our satellite we're not going to delve any deeper into the subject. A solution to the problem, that will work is to build a small pressure chamber, that holds the cell, and keeps the pressure a about 1 atm around the cell. This solution does, however, require extra material that adds to the limited weight budget.

5.4 Temperature Tests of Batteries

5.4.1 Test at Different Temperatures

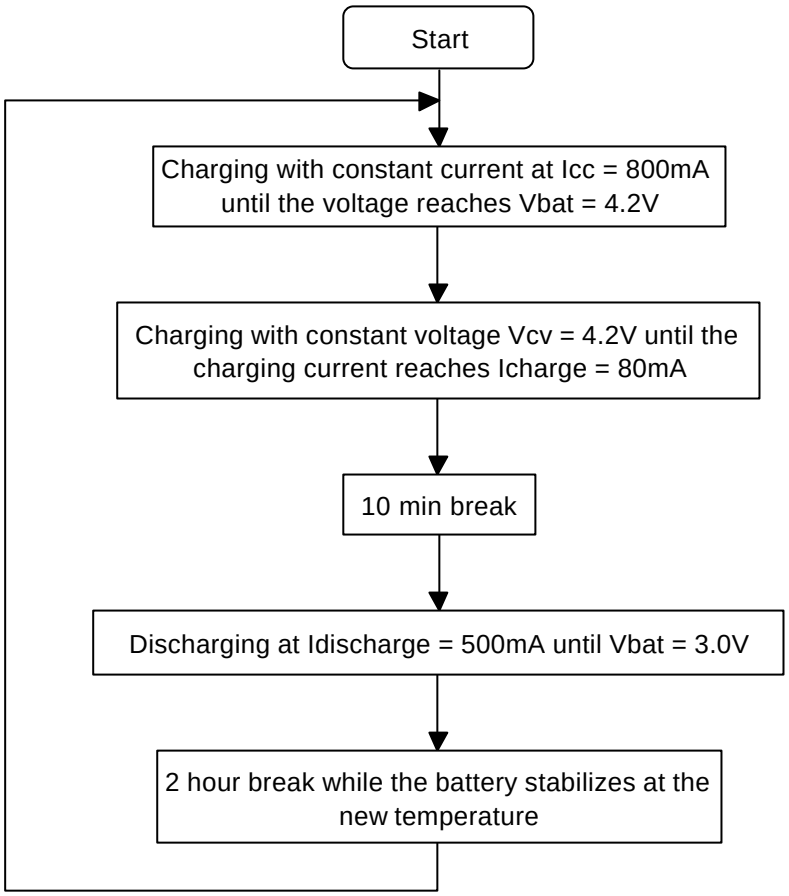
Nokia have helped us perform some temperature tests on the CGR18650H cell. We've also done a vacuum test of the cell (see section 5.3), but unfortunately we didn't have the opportunity to combine the two in one test.

In the temperature test the capacity is measured at the following temperatures, and in this order: +23 ºC, -40 ºC, -20 ºC, -10 ºC, +10 ºC, +35 ºC, +55 ºC and +23 ºC, where the last measurement at +23 ºC is to compare with the initial condition to see if the capacity has changed.

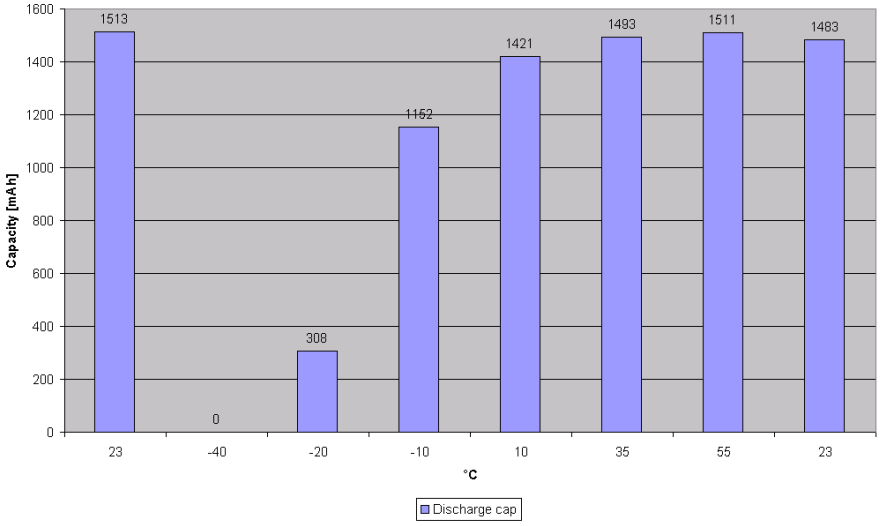
When the temperature has been stabilized a complete charge / discharge cycle has been performed at the respective temperatures. During operation in the satellite, the batteries will be charged while the solar panels are illuminated which means that the battery will be at a higher temperature, and the battery is discharged at a possible low temperature while the satellite is not illuminated.

This means that the test conditions are worse than we're going to expect. We've also done a more realistic test, which is discussed in the next section.

The charging is performed as constant current - constant voltage (as required for Li-Ion batteries) and the battery is discharged at 500mA until the voltage reaches 3V.



The results can be seen in the next figure. It can be seen that at –40 ºC the capacity is zero. This happens because at this low temperature the impedance of the battery is extremely high.



At –20 ºC the capacity is only one-fifth of the initial capacity but at –10 ºC the capacity is four-fifth. Notice that the last measurement at +23 ºC does not have the same capacity as the initial +23 ºC measurement. This is caused by the aging of the battery. The aging process is relatively larger in the start of the battery's lifetime. The aging is caused by internal chemical action which is strongly temperature dependent. The low temperatures don't provide permanent damage but high

temperatures (above 45 ºC) speed up the aging process and therefore it is urgent to prevent the battery from being too hot over long time.

5.4.2 Freezer Test

We also did a temperature test of the CGR18650H cell ourselves. It was first charged at room temperature, and then put into a freezer, operating at apx -18 °C, and discharged. The discharge curve can be seen in Appendix C.4. From the measurements it can be seen that the capacity is 4247 mWh. This is somewhat lower than what we measured at room temperature in section 5.2, namely: $\frac{4247\ \text{mWh}}{5600\ \text{mWh}} = 75{,}8\%$ of the original capacity, but this result is far better than the complete charge / discharge cycle held at -20 °C. This is because it is more difficult to charge the battery at the low temperature.

After the discharge in the freezer the battery voltage fairly quickly raises to about 3.7 V, suggesting that it holds more energy. We therefore continued the discharge at room temperature. This added additional 877 mWh, therefore the capacity totaled:

4247 + 877 mWh = 5124 mWh, that is, we've lost: $1 - \frac{5124\ \text{mWh}}{5600\ \text{mWh}} = 8{,}5\%$. This suggests that some of the energy (8,5%) is lost due to a higher internal cell impedance, and that the remaining energy (877 mWh) is simply not available because of a lower cell voltage - we stopped the discharge when the cell voltage reached 3,0 V.

6. Connections

A complete overview of the electrical interfaces of the power subsystem can be seen in Appendix D.

The following table shows the connections between Power and OBC. The connector is going to be a 28 pin 2,54 mm pitch pin header, 90°, double row. The specification of the location of pin 1 can be seen in Appendix E.

1	kill switch bypass 1	2	kill switch bypass 2
3	Unregulated bus	4	Unregulated bus
5	Ground	6	Ground
7	Regulated bus (3V3)	8	Regulated bus (3V3)
9	Latchup return signal	10	Latchup return signal
11	not used / spare	12	not used / spare
13	SPI Select 3 [1)]	14	SPI Select 4 [1)]
15	SPI Out (as seen from OBC)	16	SPI In (as seen from OBC)
17	SPI Clock	18	Sign (charging / discharging battery)
19	One wire temperature bus	20	not used / spare
21	not used / spare	22	not used / spare
23	Regulated bus (3V3)	24	Regulated bus (3V3)
25	Ground	26	Ground
27	Unregulated bus	28	Unregulated bus

[1)] Other subsystems are using SPI Select 0-2.

The power subsystem also features connections for the following components:

		Number of wires
Solar Cells	Power	5
	Ground	5
Battery	Power	1
	Ground	1
Killswitches (2 pcs)		4 x 2
Flightpin		4

It is possible that the flightpin will be soldered directly onto the Power PCB. Otherwise it will be connected by wires, soldered onto the Power PCB like the remaining connections in the above table.

7. Design

This section describes the design of the power subsystem. This includes the circuits for collecting housekeeping data, the battery charger and undervoltage protection system, and the latchup circuitry. The DC/DC converter will be designed in section 8.

Schematics and the PCB layout can be found in Appendix I and J, and in Appendix L a picture of the prototype can be seen.

7.1 Housekeeping

The housekeeping task consists of collecting the following information:

- Currents from each solar array (5),
- Common voltage for solar arrays (unregulated bus voltage),
- Battery voltage,
- Current to/from the battery,
- The regulated DC bus voltage,
- The current drawn at the regulated DC bus,
- The temperature of the battery, and possibly
- The temperature of the coils.

The temperatures are measured by means of temperature sensors featuring a Dallas one-wire system. Other groups of the DTUsat project are investigating this issue and are writing the necessary driver software for interfacing to the OBC. We will therefore not discuss this any further.

The remaining 10 currents and voltages are going to be measured by circuitry located on the Power PCB. The electrical interface to the OBC has been defined as an SPI-bus. This consists of a clock signal, a data in and out pair, and some chip select signals. Again the software for interfacing to the OBC is going to be written by another group. We have, however, written some code to test the circuits using the ISA Data Aquisition Card we developed during the first part of the project.

It should be noted that by measuring the battery temperature and voltage it is possible to estimate the remaining capacity of the battery. This may be more accurate than integrating the battery voltage and current drawn from the battery over time, since we might loose some short current bursts if we sample at a low frequency, e.g. every 10 seconds.

It is also important to note that inaccuracies (resistor values, reference voltages, etc) must be accounted for by software. This is also done in some earth applications but in those it is also common to use potentiometers. Of course that is not an option for space applications due to the dynamic environment during launch.

7.1.1 A/D Converter

We were looking for an a/d converter that could operate at 3,3V. The power consumption was required to be low (due to the limited input power from the solar cells). Optimally this could be improved by some kind of power down mode. Because of the limited amount of board space we were also looking for a build-in multiplexer and reference. Also the housing should be as small as possible, on the other hand, we can't use BGA or similar packaging for practical reasons due to soldering. Finally the electrical interface should be compatible with the SPI bus. The sampling resolution wasn't a major issue, but 10-12 bits seemed reasonable - anything higher would be overkill.

The sampling of the 10 signals could be done by using one 16 channel mux, two 8 channel muxes etc. It could also be done by using one 8 channel mux and one 2 channel mux. In the end we decided to go for two 8 channel muxes for a number of reasons. Firstly it allows for sampling of additional signals if it is found interesting at a later point, also this allows us to group the signals into two groups, one being the five currents from the solar cells, and the other group containing the remaining signals.

The reason for the segmentation is, that we might need to sample the currents from the solar cells once every second. The data will be used by the attitude control system in order to determine the location of the sun. This method has a few drawbacks, a major one being that we only have solar cells on 5 of the 6 sides of the satellite. It is therefore likely that the ACDS group will develop another solution that doesn't require the sampling of the solar cell currents.

The remaining bus voltages and currents don't need to be measured very often. This means that the a/d converter will be powered down for most of the time.

The Maxim max1281 12 bit a/d converter turned out to fulfill all our requirements. It is sold only in a 20-pin TSSOP package.

7.1.2 Measurement of Currents from the Solar Arrays

Currents are measured as voltage drops across a small resistor (tens of mΩ). A larger resistor features better accuracy, but also a larger voltage drop and power loss. Because the voltage drop is very small a current amplifier is needed. Maxim manufactures some highly integrated current amplifiers, for instance max4172 that only requires two external resistors (R_{sense} and R_{out}). The device is unidirectional meaning that the current may only flow one way through the resistor.

Having 2 cells in parallel the maximum current delivered per panel (i.e. per satellite side), at the maximum power point is:

$$I = 2 \cdot 280mA = 560mA; 600mA \text{ chosen}$$

The sense resistor is selected by trading off the accuracy against the voltage drop. A sense resistor of 51 mΩ has been chosen. V_{out} of the max4172 device is upper bounded by:

$$V_{dd} - 1,2V = 3,3V - 1,2V = 2,1V$$

The power source for the max4172 devices has been chosen as the power bus in order to protect the max 4172 from latchup conditions. Due to this low bus voltage we have to use low side current measurement. When the power is turned off the voltage across the sense resistor is at most: 51mΩ · 0,6A = 30mV, which is within the limits of the specifications of max4172.

Next R_{out} can be calculated using the following formula (from the datasheet):

$$R_{Out} = \frac{V_{Out}}{Gm \cdot R_{Sense} \cdot I_{Load}} = \frac{2,1V}{10mA / V \cdot 0,051\Omega \cdot 600mA} = 6,8\ k\Omega$$

The scaling factor is thus:

$$V_{Out} / I_{Sense} = R_{Out} \cdot R_{Sense} \cdot Gm = 6,8\ k\Omega \cdot 0,051\Omega \cdot 0,010A = 3,468\ V/A$$

The heat dissipated from R_{sense} is: $P_{sense} = R \cdot I^2 = 0{,}051\,\Omega \cdot (0{,}600\ A)^2 = 18{,}4\ mW$. This is found to be acceptable, both according to power loss, and heat dissipation in vacuum.

7.1.3 Measurements of Current to the Regulated Bus

We also use the max4172 to measure the current provided to the regulated bus. The maximum current is about 350 mA, but we'll design for 750 mA in order to have some headroom. This is, of course, a tradeoff with accuracy. Again R_{Out}, the scaling factor, and power dissipation is calculated:

$$R_{Out} = \frac{V_{Out}}{Gm \cdot R_{Sense} \cdot I_{Load}} = \frac{2{,}1V}{10mA/V \cdot 0{,}051\Omega \cdot 700mA} = 5{,}8\ k\Omega \approx 5{,}6k\Omega$$

$$V_{Out} / I_{Sense} = R_{Out} \cdot R_{Sense} \cdot Gm = 5{,}6\ k\Omega \cdot 0{,}051\Omega \cdot 0{,}010A = 2{,}856\ V/A$$

$$P_{sense} = R \cdot I^2 = 0{,}051\,\Omega \cdot (0{,}700\ A)^2 = 25{,}0\ mW$$

7.1.4 Measurements of Current to/from the Battery

For the purpose of measuring the battery current we need a current amplifier that, in contrast to max4172, is bi-directional. The max472 offers this functionality at the cost of a couple of additional external components (these adds a higher flexibility), and a slightly higher cost.

The battery is charged at up to 500 mA, and the highest discharge is 600 mA (during transmission while in shadow) - the average current is about 170 mA. We choose to add some headroom and design for a current of 1000 mA. According to the datasheet the maximum output voltage is:

$$V_{out,\,max} = V_{RS+} - 1{,}5V = 3{,}0 - 1{,}5V = 1{,}5V$$

Again we choose a sense resistor of 51 mΩ, and $R_G = R_{G1} = R_{G2}$ is set to 150Ω. Therefore R_{out} becomes:

$$R_{Out} = \frac{V_{Out} \cdot R_G}{R_{Sense} \cdot I_{Load}} = \frac{1{,}5V \cdot 150\Omega}{0{,}051\Omega \cdot 1{,}00A} = 4{,}4\ k\Omega \approx 4{,}3\ k\Omega$$

The scaling factor is thus:

$$V_{Out} / I_{Sense} = R_{Out} \cdot R_{Sense} / R_G = 4{,}3\ k\Omega \cdot 0{,}051\Omega / 150\Omega = 1{,}462\ V/A$$

The heat dissipated from R_{sense} is: $P_{sense,avg} = R \cdot I^2 = 0{,}051\,\Omega \cdot (0{,}170\ A)^2 = 1{,}5\ mW$, the highest current drawn (during transmission while the satellite is in shadow) is:
$P_{sense,max} = R \cdot I^2 = 0{,}051\,\Omega \cdot (1{,}00\ A)^2 = 51\ mW$, and the maximum voltage drop is:
$51m\Omega \cdot 1{,}0A = 51mV$. This is found to be acceptable, both according to power loss, and heat dissipation.

7.1.5 Measuring of Bus Voltages

We're also going to measure some bus voltages, all being higher than our reference of 2,5V. We therefore need some voltage dividers. The maximum input current into any of the inputs of the a/d converter is 1 µA. We therefore choose the voltage divider to supply a current of 2 µA. We need to measure the following voltages:

	min voltage	max voltage	scaling factor	max series resistance	resistors chosen (R1:R2)	actual scale	measured voltage
Unregulated bus	2,6 V	6,2 V	1:3	1,3 MΩ	430 k : 820 k	0,344	< 2,14 V
Battery	3,0 V	4,2 V	1:2	1,3 MΩ	620 k : 620 k	0,500	< 2,10 V
3,6V bus	3,6 V		3:5	1,8 MΩ	1000 k : 680 k	0,595	2,14 V
Regulated bus	3,3 V		2:3	1,6 MΩ	910 k : 510 k	0,641	2,15 V

V_{meas} o----/\/\/----o----/\/\/----o Gnd
R_2 | R_1
o adc

The scaling factors have been chosen in order to keep the measured voltage below 2,5 V with some margin. The maximum series resistance is: $R_{max} = U_{min} / 2\ \mu A$. The resistors were chosen to comply with the following two formulas:

$$R_1 + R_2 < R_{max} \quad \text{and} \quad R_1 / (R_2 + R_1) \approx \text{scaling factor.}$$

7.2 Blocking Diodes

We're going to use Schottky diodes for the blocking diodes, and for the battery diode. These feature a lower voltage drop than traditional rectifier diodes. We have chosen Phillips PRLL5817.

I_F	$V_{F, Max}$
0,1 A	320 mV
1 A	450 mV
3 A	750 mV

The power dissipation is:

Solar cells (600 mA):	$P = U \cdot I = 0{,}45V \cdot 0{,}6\ A = 270\ mW$
Battery, avg (170 mA):	$P = U \cdot I = 0{,}45V \cdot 0{,}17\ A = 75\ mW$
Battery, max (1000 mA):	$P = U \cdot I = 0{,}45V \cdot 1{,}00\ A = 450\ mW$

These results suggests that we need several diodes in parallel as the battery diode, and possibly two in parallel as blocking diodes.

7.3 Local Latchup Protection

We're going to use the max89x current limiting switch to monitor the current drawn by our a/d converters and other circuits. The power drawn by our components is rather limited, < 20 mA:

Component	Pcs	Current, max	Current, total
max4172	6	1,6 mA	9,6 mA
max1281	2	3,5 mA	7,0 mA
		Total	16,6 mA

This suggests that we use the max892, that features an internal resistance of max 500 mΩ, and a maximum current limit of 250 mA. This results in a maximum voltage drop of 1 mV, which is found acceptable.

When we set the current limit threshold we use a somewhat higher current value. This is due to the fact that the current drawn from the circuits may rise when they are exposed to radiation. This higher current limit is fine in regard to latch up detection, because this event causes a short circuit that will cause a far higher current to flow. For now we use a threshold of 75 mA:

$$R_{Set} = 1240\ V / I_{Set} = 1240\ V / 0{,}075\ A = 16{,}5\ k\Omega \approx 16\ k\Omega$$

7.4 Undervoltage Protection

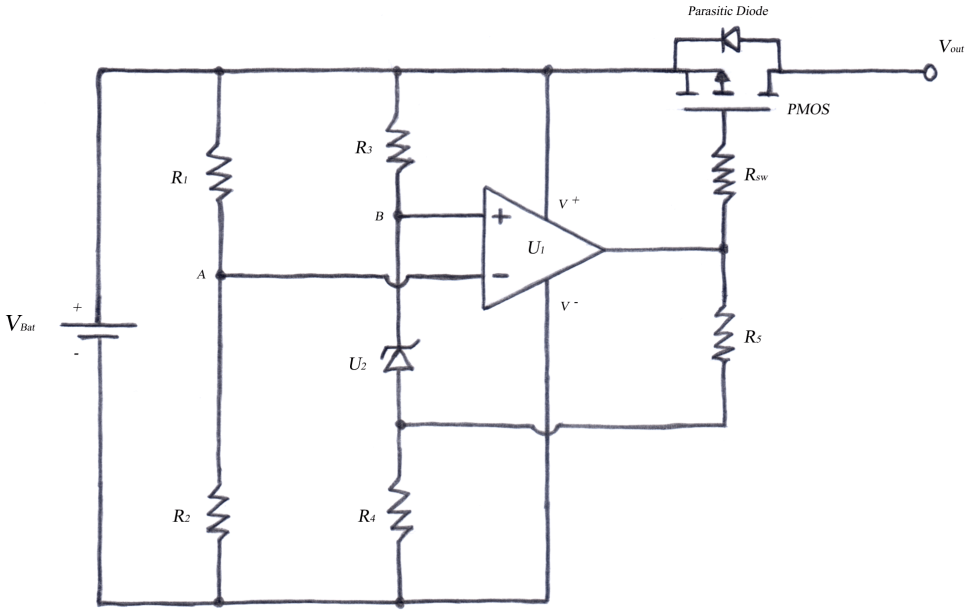
If a Li-Ion battery is discharged below its end of discharge voltage, V_{end}, the battery can be damaged, so it is extremely urgent that this event never occurs. Therefore a battery protection circuit is needed.

When designing the protection two demands must be fulfilled:

- The protection circuit must be able to disconnect the battery from the load to prevent deep discharge of the battery when the battery voltage drops below V_{End}.
- The protection circuit must consume as little power as possible, so the circuit doesn't drain the battery while it is disconnected from the load.

A single chip solution for undervoltage protection of Li-Ion batteries can be used but these are built in CMOS technology so a latch up can occur. There is no latch up protection between the battery and the undervoltage protection circuit, so if a latch up occur it will destroy the protection circuit, and possibly drain the battery completely. This will cause the satellite to stop working.

To make the protection circuit latch up free a design where only bipolar technology is used is needed. The following will describe a circuit in bipolar technology that will protect the battery and fulfill the demands above. The protection circuit is shown below.



As long as the battery voltage V_{bat} is above the end of discharge voltage V_{end} the PMOS will be turned on, when V_{bat} falls below V_{end} the PMOS will turn off.

When the battery voltage falls below V_{end} the battery is disconnected from the load. This allows the battery voltage to rise above V_{end} causing the PMOS to turn on. Now the battery is again loaded, and the battery voltage will drop below V_{end} causing the battery to be disconnected again. To avoid this kind of oscillation some hysteresis is introduced.

Notice the PMOS parasitic diode on the figure, this parasitic diode will always be blocking so it will not cause uncontrolled discharge of the battery.

Because the MOS switch is on the high side of the battery only a PMOS transistor is preferred to be used for the switch.

Now a more detailed description of how the circuit really works will be discussed. At node A the voltage is:

$$V_A = V_{Bat} \cdot \frac{R_2}{R_2 + R_1}$$

To find the voltage at node B, Kirchoff's current law is applied to node x and the voltage at node x is found to be:

$$0 = \frac{V_{out,op-amp} - V_X}{R_5} + \frac{V_{bat} - V_{u2} - V_X}{R_3} - \frac{V_X}{R_4}$$

$$V_X = \frac{\frac{V_{bat} - V_{u2}}{R_3} + \frac{V_{out,op-amp}}{R_5}}{\frac{1}{R_3} + \frac{1}{R_4} + \frac{1}{R_5}}$$

Where $V_{out,op\text{-}amp}$ is zero under battery discharge and $V_{out,op\text{-}amp} = V_{bat}$ under battery shot down, because it is assumed that the op amp is rail to rail.

The voltage at node B:

$$V_B = V_{u2} + V_X$$

The output V_{out,op_amp} of the operational amplifier U_1 is determined as

$$V_{out,op\_amp} = G\left(V_{in,+} - V_{in,-}\right) = G\left(V_B - V_A\right)$$

Where G is the gain of the op amp. It can now be seen that as long as

$$V_A > V_B \Rightarrow V_{out,op\_amp} = V_- = 0$$
$$V_A < V_B \Rightarrow V_{out,op\_amp} = V_+ = V_{Bat}$$

The values of the resistors and U_2 must have a size that causes V_A to be larger than V_B as long as the battery voltage V_{bat} is larger than the end of discharge voltage V_{end}.

This means that when

$V_{Bat} > V_{End} \Rightarrow V_A > V_B \Rightarrow V_{out,op\_amp} = 0$ and this turns on the PMOS.

$V_{Bat} < V_{End} \Rightarrow V_A < V_B \Rightarrow V_{out,op\_amp} = V_{Bat}$ and this turns off the PMOS.

When the output of the op amp U_1 gets high the voltage of node B is added some extra potential from the current in R_5. This extra potential is found as the voltage at node B, $V_{B,high}$, when the output of the op amp is high, minus the voltage at node B, $V_{B,low}$, when the output of the op amp is low.

$$V_{B,added} = V_{B,high} - V_{B,low} = \frac{V_{bat}/R_5}{\frac{1}{R_3}+\frac{1}{R_4}+\frac{1}{R_5}}$$

The hysteresis for the circuit determines how much the battery voltage must rise again in order to allow discharge of the battery after a temporally shutdown.

The voltage that the battery must rise to, in order to allow discharge of the battery after a temporally shutdown after that the battery voltage have decreased to the end of discharge voltage V_{end} is called $V_{bat,rise}$. This $V_{bat,rise}$ can be found by looking at how much the battery voltage must rise in order to make the potential V_A at node A higher than the potential $V_{B,high}$ at node B.

$$V_A > V_{\mathbf{B},high} \Leftrightarrow$$

$$V_{bat} \cdot \frac{R_2}{R_1+R_2} > \frac{\frac{V_{bat}-V_{u2}}{R_3}+\frac{V_{out,op-amp}}{R_5}}{\frac{1}{R_3}+\frac{1}{R_4}+\frac{1}{R_5}} + V_{u2} \Leftrightarrow$$

$$V_{bat,rise} = V_{bat} > \frac{\frac{-V_{u2}}{R_3\left(1/R_3+1/R_4+1/R_5\right)} + V_{u2}}{\frac{R_2}{R_1+R_2} - \frac{1}{R_3\left(1/R_3+1/R_4+1/R_5\right)} - \frac{1}{R_5\left(1/R_3+1/R_4+1/R_5\right)}}$$

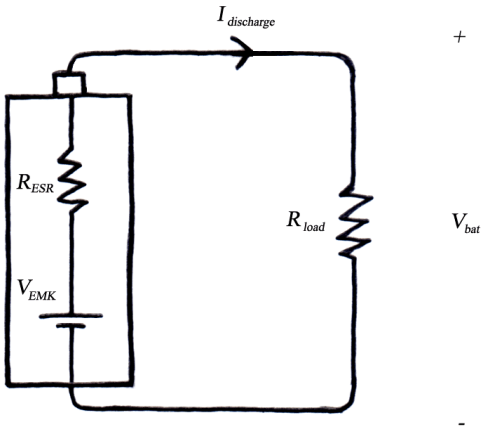
The hysteresis $H_{bat,protection}$ for the protection circuit can be found as the voltage $V_{bat,rise}$ minus the end of discharge voltage V_{end}.

$$H_{bat,protection} = V_{bat,rise} - V_{End}$$

The resistance R_{sw} prevents large peak currents in the gate because it introduces a time constant to the gate capacitance.

7.4.1 The Battery Hysteresis

To understand why the battery voltage rises when it is unloaded we have to look at how a battery works. A chemistry independent battery is shown in the figure below.



A battery can be seen as an electromotive force V_{EMK} in series with an equivalent series resistance R_{SER}. The electromotive force can be described as

$$V_{EMK} = (R_{ESR} + R_{load}) \cdot I_{discharge}$$

And now the battery voltage V_{bat} can be expressed as

$$V_{bat} = R_{load} \cdot I_{discharge} = V_{EMK} - R_{ESR} \cdot I_{discharge}$$

When no load is connected to the battery, no current will flow, $I_{discharge} = 0$, and the battery voltage will climb back to $V_{bat} = V_{EMK} - R_{ESR} \cdot 0 = V_{EMK}$

Therefore the minimum hysteresis needed to avoid oscillation is

$$H_{\min} = R_{ESR} \cdot I_{discharge}$$

7.4.2 Component Values for the Undervoltage Protection Circuit

The components used for the undervoltage protection circuit can be seen in the table below.

R_1 = 3.57 MΩ	R_5 = 10MΩ
R_2 = 3.00 MΩ	R_{sw} = 1MΩ
R_3 = 2.05 MΩ	U_1 = LT1494
R_4 = 150 kΩ	U_2 = LT1389 with V_{u2} = 1.25V

7.5 Shunt Regulator

When the electronic circuits are disconnected from the solar cells a high voltage level may occur. If some electronic circuits can't cope with this high voltage they might be destroyed. Because of the electrical characteristics of the solar cells even a small (couple of mA) will lower the output voltage to an acceptable level.

Normally one would use a resistor in series with a zener diode to limit the voltage, but because of the small currents we're working with we can skip the resistor and only use a zener diode. This diode is clamping the maximum voltage level of the unregulated bus.

7.6 Battery Charger

The Maxim max1879 Li-Ion battery charger requires a 100 nF capacitor at the In pin. The battery is bypassed by a 2,2 uF capacitor - Maxim recommends 1,5 uF per amp of charge current (we charge with at most 0,5 A). The thermistor is replaced by a 10 kΩ resistor because we don't want to use a temperature sensor.

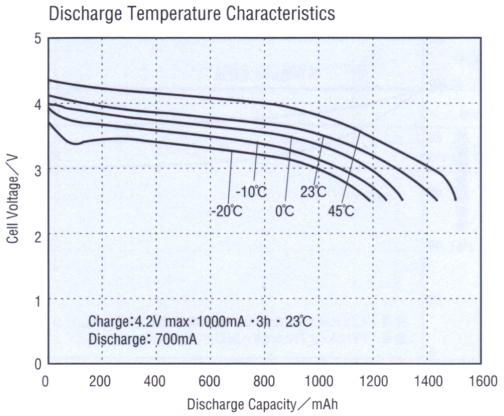
Finally the ADJ pin must be bypassed by a 1nF capacitor, and TSEL is connected to the positive battery terminal in order to set the minimum on-time in top-off to 34 ms (smallest value possible).

The P-MOS transistor is the SI9803DY from Vishay.

7.7 Battery Heating

When the satellite enters the shadow the battery may become very cold because of the satellites small size. When discharging a Li-Ion battery at temperatures below -20 °C the internal impedance of the battery is so high that the capacity of the battery becomes very low.

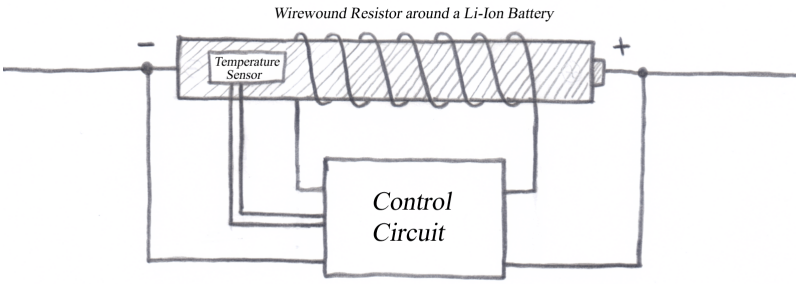
A typical discharge curve for a Li-Ion battery is shown in the figure below:



It can be seen that for the -20 °C curve the voltage decreases rapidly in the beginning and then increases again. The decrease is caused by the high internal battery impedance and when current is drawn from the battery the internal chemical activity causes a temperature rise which decreases the impedance and makes the voltage rise again. This phenomena would be even clearer if the temperature curve for -30 °C was shown.

The internal battery heating caused by chemical activity when current is drawn from the battery could be extended to external battery heating to achieve larger battery capacity at these low temperatures. Of course the energy used to heat the battery should be small, as it will only be useful if we gain capacity even though we spend some energy on heating.

In order to reduce the required energy to heat the battery the battery, and heating control circuit can be placed inside some insulation. For space applications Multi Layer Insulating foil (MLI) is a very effective isolator. This reduces heat radiation to almost zero and the only heat loss would be through the wires from the battery terminals to the PCB.



A possible solution is shown in the figure above. The control circuit could be a low power comparator (the heat it dissipates will help heat the battery) that could turn on the wirewound resistor when needed.

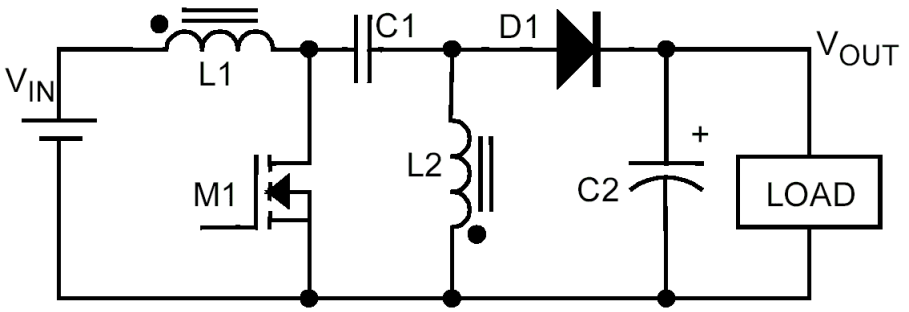
8. DC/DC Converter

This section describes the design of the DC/DC converter. Schematics and the PCB layout can be found in Appendix I and J, and in Appendix L a picture of the prototype can be seen.

8.1 SEPIC Converters

The SEPIC (Single Ended Primary Inductor Circuit) can produce a regulated output voltage even though the input voltage may be lower or higher than the output voltage. The SEPIC converter does not invert the output like the CUK and Flyback converter.

This is just what is needed for our purpose. The SEPIC configuration is shown below.

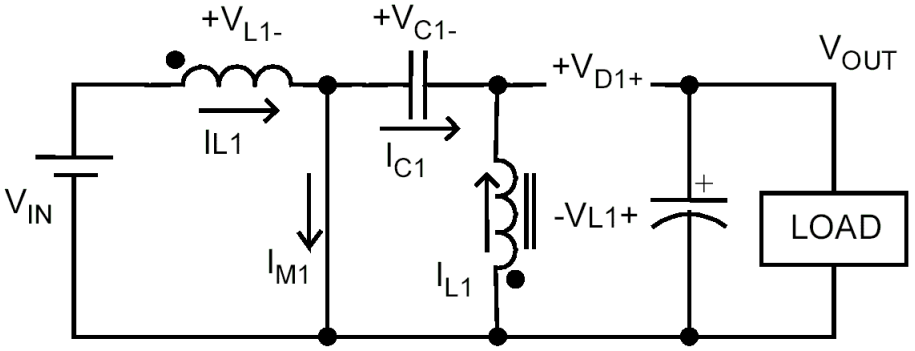


To increase efficiency the two inductors are wound on the same core. When the two inductors are wound on the same core they will not act as two discrete inductors, but as a transformer because of the mutual inductance. Because we use the same inductance value for the two inductors and that the voltage in steady state across the two inductors is the same (explained later) we can assume that the coupled inductors will behave like two discrete inductors like the ones shown in the above figure.

In the following a description of how the SEPIC circuit works will be given. The circuit have two modes, the MOSFET M1 can either be on or off.

Mode 1: ($0 < t < t_{on}$) M1 is on

When M1 is on it will act as a short circuit if we neglect its on resistance. The diode D1 will be reverse biased and assumed to be an open circuit. The SEPIC circuit in the on state is shown below.



The input voltage V_{IN} is across the inductor L_1 and the current in L_1 increases in linear proportion.

$$V_{L1} = L\frac{dI_{L1}(t)}{dt} \quad \Leftrightarrow \quad I_{L1} = \frac{1}{L}\int V_{L1}(t)\,dt \quad \Rightarrow \quad I_{L1} = \frac{1}{L}\cdot V_{IN}\cdot t$$

The voltage across L_2 is the voltage V_{C1} of C_1. In steady state the average voltage across an inductor is zero if we neglect the resistance of the inductor. This means that the average voltage V_{C1} of capacitor C_1 is the same as the input voltage V_{IN}. Actually the voltage of C_1 will vary around the V_{IN} voltage as can be seen on the plots of voltages, shown later.

Because the two inductors have the same inductance and that we have assumed that $V_{IN} = V_{C1}$ the two currents in the inductors will also be equal.

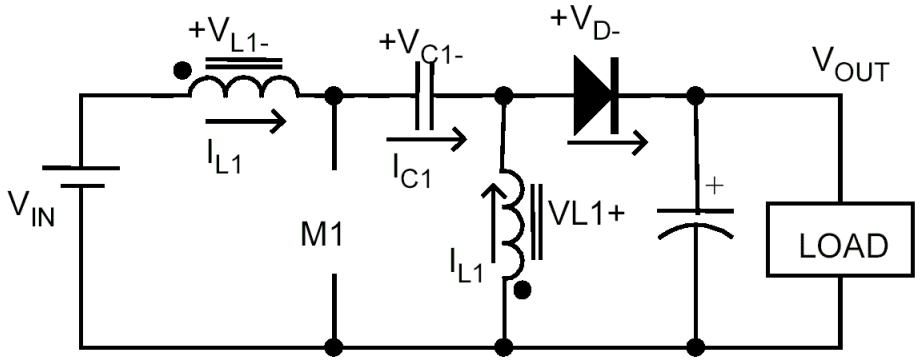
$$I_{L2} = \frac{1}{L} \cdot V_{C1} \cdot t = \frac{1}{L} \cdot V_{IN} \cdot t = I_{L1}$$

The energy stored in the two inductors are also equal and are given by

$$E_{L_1} = E_{L_2} = 1/2 \cdot L \cdot i_L^2 = 1/2 \cdot (V_{IN} \cdot t)^2$$

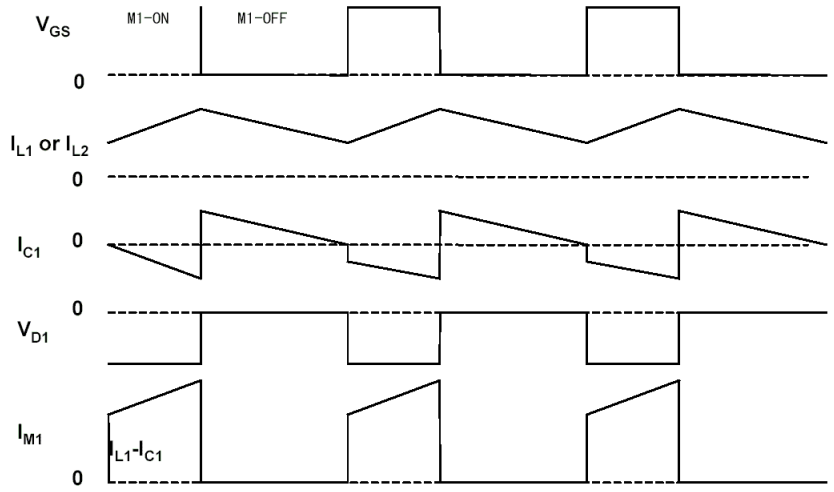
Mode 2: (t_{on} < t < T) M1 is off

When M1 is off it will act as an open circuit, the diode D1 will be reversed biased. The circuit in the off mode is shown below.



The magnetic energy stored in inductor L_1 is used to charge capacitor C_1, and the energy stored in L_2 is charging the output capacitor C_2. The forward diode voltage drop is neglected. The diode could be replaced by a MOSFET to increase efficiency, but it is very urgent that the two MOSFETs never are on at the same time if it happens the output of the converter will be grounded.

The currents in the SEPIC converter operated in CCM are shown in the current plot on the next page.

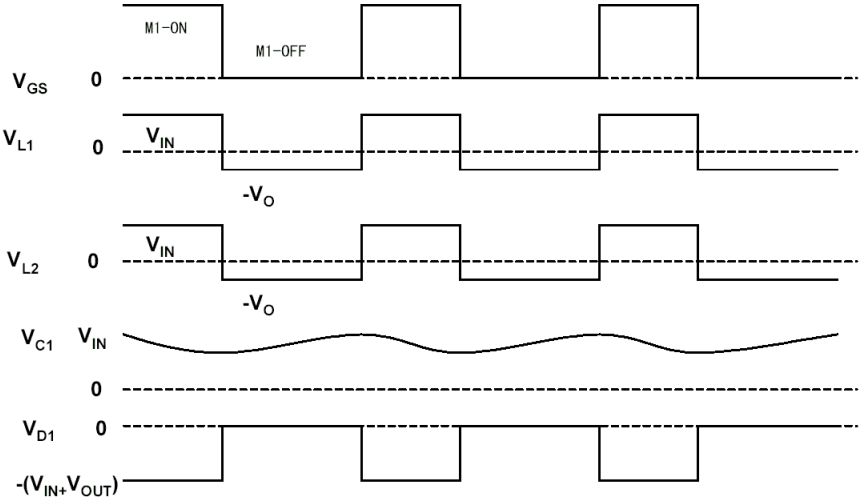


The voltage V_{GS} just shows the on and off periods of M1 and the diode voltage V_{D1} show when the diode is reversed and forward biased. The current in the two inductors I_{L1} and I_{L2} increases linearly in the on period and decreases linearly in the off period.

The capacitor current I_{C1} is as shown.

The current M1 is the sum of the inductor and capacitor current. The peak current of I_{M1} is the same as the total peak current in the coupled inductor, so it is this peak current that must flow in the inductor without the core material enters saturation.

The voltages in the converter are shown below



In the on period the voltage across the inductors are equal to V_{IN} and in the off period the inductor voltages are equal to minus the output voltage because we neglect the diode forward voltage drop.

The capacitor voltage V_{C1} will vary around the input voltage as shown. The reversed diode voltage is V_{IN} plus V_{OUT}.

In the steady state there must be voltage-second balance for the inductor, so the voltage area for the on period must be equal to the voltage area for the off period.

$$V_{IN} \cdot DT - V_{OUT} \cdot (1-D) \cdot T = 0$$

The transfer function for the SEPIC converter can now be calculated to be

$$\frac{V_{OUT}}{V_{IN}} = \frac{D}{1-D}$$

8.2 SEPIC Converter Design

Now that we have described the SEPIC topology it is time to do some actual design. We'll start to summarize the demands of the circuit:

Input Voltage (min)	2,6 V
Input Voltage (bat,max)	3,8 V
Input Voltage (max)	6,0 V

Output Voltage	3,6 V
Output Current (max)	0,7 A

Frequency	100 kHz

R_{Cp}	0,05 Ω
R_{sw}	0,06 Ω

$R_{L1} = R_{L2}$	0,12 Ω

First we note that at equilibrium the DC voltage across the two inductors L1 and L2 is zero. Therefore Cp sees a DC potential of V_{In} through L1, and ground through L2. The DC voltage across Cp is thus:

$$V_{Cp,\,mean} = V_{In} \leq 6{,}0\ V$$

Let T be the period of one switching cycle, and let d be the dutycycle, then $T_{On} = T \cdot d$ is the portion of T for which the switch Sw1 is closed. The switch is open for the remaining $T_{Off} = T \cdot (1-d)$ part of the period. The second switch, Sw2, is operating in antiphase with Sw1, except for a short time at the transitions when both switches are turned off.

The voltage across L1 equals zero during steady-state conditions. This implies that the voltage seen during T_{On} is exactly compensated by the voltage seen during T_{Off}. We have:

$$d \cdot T \cdot V_{In} = (1-d) \cdot T \cdot (V_{Out} + R_{Sw2} \cdot I_{Out} + V_{Cp} - V_{In}) = (1-d) \cdot T \cdot (V_{Out} + R_{Sw2} \cdot I_{Out})$$

Where $V_{Cp} = V_{In}$, as shown above. This can be rewritten to:

$$(V_{Out} + R_{Sw2} \cdot I_{Out})/V_{In} = d/(1+d) = A_{Ideal}$$

where A_{Ideal} is the ideal amplification factor. This means that all parasitic resistances are neglected. It is now obvious that the output voltage can become both smaller and larger than the input voltage, depending on the dutycycle A_{Ideal}. This is, of course, the main reason that we want to use a SEPIC converter.

If we include the parasitic resistances in the circuit we get:

$$A_{Actual} = (V_{Out} + I_{Out} \cdot R_{Sw2} + I_{Out} \cdot (A_{ideal} \cdot R_{Cp} + R_{L2}))/(V_{In} - A_{Ideal}(R_{L1} + R_{Sw1}) \cdot I_{Out} - R_{Sw1} \cdot I_{Out})$$

It should be noted that the formula is recursive, but only a few iterations provides a reasonably accurate result. We can now use this formula to calculate the actual amplification factors for different input voltages. In our case 2,6V, 3,8V, and 6,0V are of interest (minimum battery voltage, maximum battery voltage, and solar cell voltage):

V_{In}	A_{actual}
2,5	1,605494
3,8	1,037206
6,0	0,637724

The above amplification factors can be used to determine the dutycycles by rewriting equation 2 to:

$$d = A / (1+A)$$

V_{In}	A_{actual}	dutycycle, d
2,5	1,605494	0,616196
3,8	1,037206	0,509132
6,0	0,637724	0,389397

Since the DC current through Cp is zero, the mean output current can only be supplied by L2:

$$I_{Out} = I_{L2} = 0,7 \text{ A}$$

Therefore the mean current into L2 does not depend on the input voltage, but only the current supplied to the load.

We can now calculate the current into L1. Again we can use the fact that no DC current can flow through Cp. Therefore the coulomb charge flowing during T_{On} is perfectly matched by an opposite coulomb charge during T_{Off}. When switch 1 is closed during T_{On} the node A potential is fixed at 0V. Since $V_{Cp,\ mean} = V_{In}$, the node B potential is -Vin. This reverse biases D1 (switch 2 will be open) while IL1 flows through Cp: $d \cdot I_{L2} = (1-d) \cdot T \cdot I_{L1}$, since $I_{L2} = I_{Out}$ we get:

$$I_{L1} = A_{Actual} \cdot I_{Out}$$

V_{In}	I_{L1}
2,5	1,123846
3,8	0,726044
6,0	0,446407

It is noted that I_{L1} depends strongly on V_{In}, because $P_{In} = P_{Out}$/Efficiency. That is, for a given output power I_{L1} increases if V_{In} decreases. Knowing that $I_{L2} = I_{Out}$ flows into Cp during T_{On} we choose Cp so that its ripple ΔV_{Cp} becomes a small fraction of V_{Cp}, in the order 1% - 5%. The worst case occurs when V_{In} is minimal:

$$Cp >= I_{Out} \cdot d_{Min} \cdot T/(5\% \cdot V_{In,min})$$

$$Cp >= 33 \text{ uF}$$

The capacitor Cp should, of course be non-polarized. This is, unfortunately a rather large value for a non-polarized capacitor, but Murata manufactures a 22uF, 10V ceramic capacitor, which we expect to use. Two of these in parallel will do fine. The voltage rating is respected, since: $V_{Cp,mean} = V_{In}$.

The power dissipation P_{Cp}, due to its own internal resistance, R_{Cp} becomes:

$$P_{Cp} = A_{actual,\ min} \cdot R_{Cp} \cdot I_{Out}^2$$
$$P_{Cp} \leq 39\ mW$$

The power dissipation of the switches results in the following losses:

$$P_{Sw} = A_{Actual,min} \cdot (1+A_{Actual,min}) \cdot R_{Sw} \cdot I_{Out}^2$$
$$P_{Sw} \leq 123\ mW$$

Also the losses in the coils can be calculated:

$$P_{RL1} = A_{Acutal,min}^2 \cdot R_{L1} \cdot I_{Out}^2$$
$$P_{RL1} \leq 151\ mW$$

$$P_{RL2} = R_{L2} \cdot I_{Out}^2$$
$$P_{RL2} \leq 60\ mW$$

The inductor L1 is chosen so its total current ripple is a fraction (k=20% to 50%) of I_{L1}. The worst case occurs when V_{In} is maximum because $d \cdot I_{L1}$ is maximum when I_{L1} is minimum:

$$L1_{min} = T \cdot (1-d_{max}) \cdot V_{In,max}/(I_{Out} \cdot 0,5)$$
$$L1_{min} = 105\ uH$$

We further need to now the saturation current, in order to be able to design the coil:

$$I_{L1,sat} >> I_{L1} + 0,5 \cdot \Delta I_{L1} = A_{Actual,min} \cdot I_{Out} + 0,5 \cdot T \cdot d_{min} \cdot V_{In,min}/L1$$
$$I_{L1,\ pulse} \leq 1,9\ A$$
$$I_{L1,\ avg} \leq 0,7\ A$$

The similar calculations for L2 are:

$$L2_{min} = T \cdot d_{max} \cdot V_{In,max}/(IOut \cdot 0,5)$$
$$L2_{min} = 67\ uH$$

$$I_{L2,sat} >> I_{L2} + 0,5 \cdot \Delta I_{L2} = I_{Out} + 0,5 \cdot T \cdot d_{max} \cdot V_{In,max}/L2$$
$$I_{L2} \leq 820\ mA$$

If the two coils are wounded on the same core (as in our case) the larger of the two values must be chosen. This is necessary because the number of turns must be the same for the two coils. Otherwise the voltages across the two windings will differ, and Cp will act as a short circuit to the difference. If the winding voltages are identical, they generate equal and cumulative current gradients.

Thus, the natural inductance of each winding should equal only half of the value calculated for L1 and L2.

The purpose of the output capacitor (C_{Out}) is to average the current pulses supplied by D1 during T_{Off}. The current transitions are brutal (similar to the flyback topology), so C_{Out} should be a high-performance capacitor, for instance a tantalium, low ESR capacitor. The minimum value for C_{Out} is determined by the amount of ripple (ΔV_{Out}) that can be tolerated:

$$C_{Out} >= A_{Actual,min} \cdot I_{Out} \cdot d_{min} \cdot T / \Delta V_{Out}$$
$$C_{Out} >= 138 \text{ uF}$$

If the load current is composed of high-energy pules the output capacitor must be much larger. Due to the filtering properties of the SEPIC topology the input capacitor can be much smaller:

$$C_{In} = C_{Out} / 10$$
$$C_{In} = 14 \text{ uF}$$

Finally the overall efficiency can be estimated from V_{In}, and A_{Actual}. The result is optimistic, because it doesn't account for switch-transition losses, core losses, or the energy used to power the controller.

$$\text{efficiency} = V_{Out} / (A_{Actual} \cdot V_{In})$$

V_{In}	A_{Actual}	Efficiency (%)
2,5	1,605494	86,2
3,8	1,037206	91,3
6,0	0,637724	94,1

Finally the switch, Sw1, should be rated for breakdown voltages greater than V_{DS}:

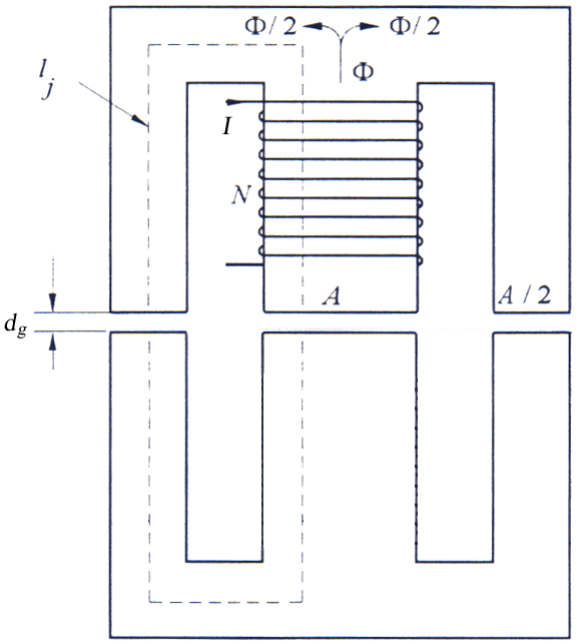
$$V_{DS} > 1{,}15 \cdot (V_{Out} + V_{In})$$
$$V_{DS} > 15 \text{ V}$$

8.3 Coils ‘n Cores

We’re now going to design the coupled inductors.

8.3.1 Magnetic Theory for the RM-Core

The RM-core is assumed to be equivalent to that shown below.

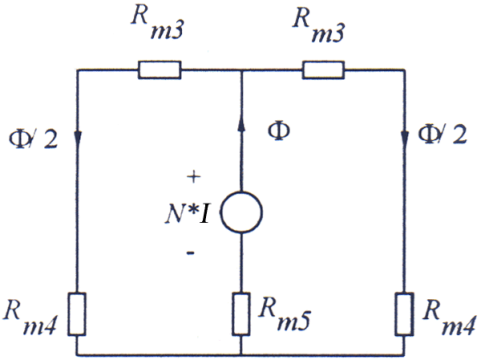


Where

- l_j is the magnetic path through the ferrite
- The cross section area of the center leg is A
- The cross section area of the outer legs is A/2
- d_g is the separation gab distance between the two core halves
- ϕ is the magnetic flux in the core
- N is the number of turns in the inductor
- I is the current through the inductor
- δ is the air gab of the core, not shown in the figure

It is further assumed that the core and the air gabs have the same respective cross section areas and that the magnetic flux is constant in the air gab if the fringing of the magnetic field at the edges of the core is neglected.

To make it easier to derive the theory for the magnetic circuit an electrical equivalent diagram is used. Here magnetic flux is equivalent to electrical current, the magnetic reluctance is equivalent to electrical resistance and magetomotive force(N · I) is equivalent to electrical voltage. The electrical equivalent diagram is shown to the right.



Here the R_{m3} is the reluctance in the two outer legs, R_{m4} is the reluctance in the two air gabs for the outer legs and R_{m5} is the reluctance in the air gab for the center leg.

The reluctances are defined as

$$R_{m3} = \frac{2l_j}{\mu_0 \mu_{r,core} A} \qquad R_{m4} = \frac{2d_g}{\mu_0 A} \qquad R_{m5} = \frac{d_g}{\mu_0 A}$$

Where $\mu_0 = 4\pi \cdot 10^{-7}$ H/m is the vacuum permeability

If the analogy for electrical current and voltage is used with Kirchoff's voltage law we get:

$$NI = \Phi R_{m5} + \Phi/2 * (R_{m3}\ R_{m4})$$

$$NI = \Phi \frac{d_g}{\mu_0 A} + \Phi/2 \left(\frac{2l_j}{\mu_0 \mu_{r,core} A} + \frac{2d_g}{\mu_0 A} \right)$$

$$NI = \Phi \left(\frac{2d_g}{\mu_0 A} + \frac{l_j}{\mu_0 \mu_{r,core} A} \right)$$

The flux Φ is isolated to:

$$\Phi = \frac{NI}{\frac{2d_g}{\mu_0 A} + \frac{l_j}{\mu_0 \mu_{r,core} A}} = \frac{NI\,\mu_0 A}{2d_g + \frac{l_j}{\mu_{r,core}}}$$

The above equation is multiplied by N and divided by I to get the inductance:

$$L = \frac{\Phi N}{I} = \frac{N^2 * \mu_0 A}{2d_g + l_j / \mu_{r,core}}$$

The gab separation distance d_g and the number of windings N can now be expressed as

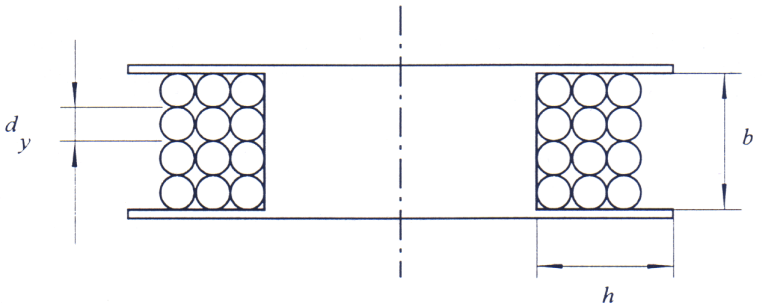
$$d_g = \frac{1}{2} \left(\frac{N^2 \mu_0 A}{L} - \frac{l_j}{\mu_{r,core}} \right) \qquad N = \sqrt{\frac{L(2d_g + l_j/\mu_{r,core})}{\mu_0 A}}$$

Because $d_g = ½\ \delta$ the air gab length δ and the number of windings N can be expressed as

$$\delta = \left(\frac{N^2 \mu_0 A}{L} - \frac{l_j}{\mu_{r,core}} \right) \qquad N = \sqrt{\frac{L(\delta + l_j/\mu_{r,core})}{\mu_0 A}}$$

8.3.2 Theory of Coil Winding

The coil is wound on a plastic coil former like the one shown on here:



The largest outer diameter d_y of the copper wire is determined by the available winding space A_v = b·h. To account for all the air between the windings, the wire is assumed to be quadratic with a side length equal to the outer diameter of the copper wire. Then the available winding space can be used to find the largest outer diameter of the wire:

$$A_v = N * d_y^2 \;\Rightarrow\; d_{y,\max} = \sqrt{\frac{A_v}{N}}$$

For a coupled inductor consisting of two inductors we get:

$$A_v = 2N * d_y^2 \;\Rightarrow\; d_{y,\max,coupled} = \sqrt{\frac{A_v}{2N}}$$

The number turns per layer is:

$$n_{turns} = \frac{b}{d_y} - 1$$

where the minus one appears because in order to make the first winding the wire must cross and this takes up an extra turn.

The maximum number of available layers for a coupled inductor consisting of two inductors that can be made on the coil former is determined by:

$$n_{layer,\max} = \frac{h/2}{d_y}$$

The number of layers needed for the coil is:

$$n_{layers,needed} = \frac{N}{n_{turns}}$$

8.3.3 Choice of Core

We have to find a core that can realize the inductance L under the following demands:

- The inductor have to be able to store the energy needed
- The temperature in the coil may never exceed T_{max}
- The core material must never enter saturation

If the temperature exceed T_{max} the lacquer insulation around the copper wire will be damaged and the inductor is destroyed. When the temperature exceed the curie temperature for the core material it will loose its ferromagnetic characteristics and the inductance of the coil will decrease very fast. The coil will also loose its ability to store energy if the core material enters saturation.

8.3.4 Core saturation

Faraday's law of electromagnetic induction states that the electromotive force (the voltage) induced in a stationary closed circuit is equal to the negative rate of the increase of the magnetic flux linking the circuit. The negative sign means that the induced voltage will cause a current to flow in the opposite direction of the linking magnetic flux [cheng].

$$\boldsymbol{n} = -\frac{d\Phi}{dt}$$

We don't need to know in what direction the current will flow so we neglect the minus sign. If the circuit consists of N turns the induced voltage will be

$$\boldsymbol{n}(t) = N\frac{d\Phi}{dt} = NA\frac{dB(t)}{dt}$$

Where A is the cross section area of the core.

The inductor current can be determined as

$$i(t) = \frac{1}{L}\int \boldsymbol{n}(t)\,dt = \frac{1}{L}\int NA\frac{dB(t)}{dt}\,dt = \frac{NAB(t)}{L}$$

To avoid that the core enters saturation the maximum magnetic field strength may not exceed the saturation value B_{sat} anywhere in the core, and therefore the smallest cross sectional area A_{min} must be used.

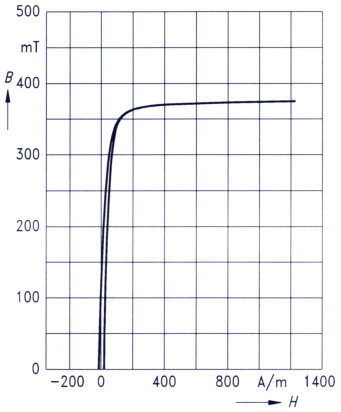
The maximum magnetic field strength B_{max} is isolated to:

$$B(t) = \frac{Li(t)}{NA} \Rightarrow B_{max} = \frac{Li_{max}}{NA_{min}}$$

The BH-magnetization curves for the N87 core material at a temperature of 100 °C are shown in the figure below. At higher temperatures the saturation of the core is lower so the curve can also be used at lower temperatures.

It can be seen that the core is in saturation at B = 375mT but the curve starts to bend already at B = 200mT.

If we set B_{sat} = 180mT there is a good security margin.



8.3.5 Core Losses

The loss in the ferrite core is determined by

$$P_{fe,core} = V_{core} \cdot C_p \left(\frac{f}{f_0} \right)^{C_f} \cdot \left(\frac{B}{B_0} \right)^{C_b}$$

Where

V_{core} : Core volume
C_p : Loss factor of the ferrite type
C_f : Frequency exponent of the ferrite type
C_b : B-field exponent of the ferrite type
f_0 : Reference frequency that the constant C_f referees to
B_0 : Reference magnetic field strength that C_p referees to

We will use the ferrite Core material N87, the volume core losses versus AC field flux density and the volume core losses versus frequency is shown in the following figures.

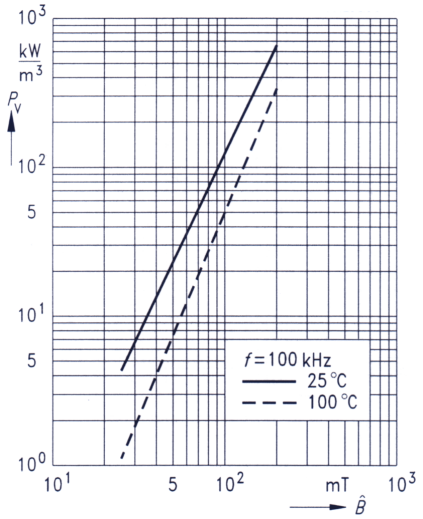


Figure A: Determines constants C_p and C_b

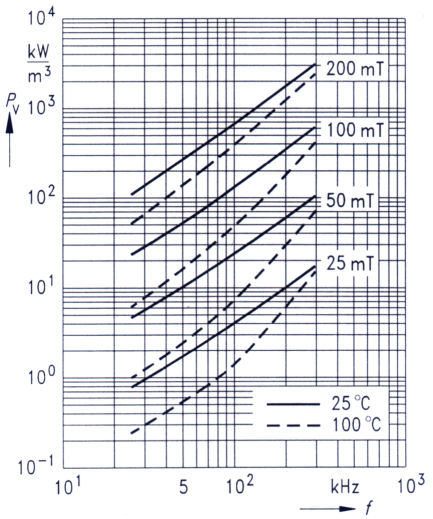


Figure B: Determines constant C_f

The constants C_p , C_f and C_b are determined at f_0 = 100kHz, B_0 = 100mT and at a core temperature of 25 °C.

From figure A the constants C_p and C_b are read to be:

$$C_p = 130 kW / m^3$$

$$C_b = \frac{\log(P_{v2}) - \log(P_{v1})}{\log(B_2) - \log(B_1)} = \frac{\log(600 kW/m^3) - \log(6.5 kW/m^3)}{\log(200 mT) - \log(30 mT)} = 2.39$$

From figure B the constant C_f is read to be

$$C_f = \frac{\log(P_{v2}) - \log(P_{v1})}{\log(f_2) - \log(f_1)} = \frac{\log(650 kW/m^3) - \log(40 kW/m^3)}{\log(300 kHz) - \log(40 kHz)} = 1.73$$

8.3.6 Copper Losses

The current through the coil I_l gives some losses and this current is a sum of a dc-component and an ac-component.

Before we can calculate the losses we have to calculate the length of the copper wire.

$$l_{wire} = n_{turns} \cdot \sum_{i=0}^{n-2} \pi (d_{coilformer} + d_y + i \cdot 2 d_y) + n_{last\_layer} \cdot \pi (d_{coilformer} + d_y + (n-1) d_y)$$

where $d_{coilformer}$ is the diameter of the coilformer , d_y is the outer diameter of the copper wire and $n_{last\text{-}layer}$ is the number of turns in the last layer.

8.3.7 DC- copper loss

The dc-component I_0 gives a dc power loss in the copper wire with the resistance R_{wire} determined by

$$P_{cu,dc} = R_{wire} \cdot I_0^2 = \rho_{cu} \cdot \frac{l_{wire}}{A_{cu}} \cdot I_0^2$$

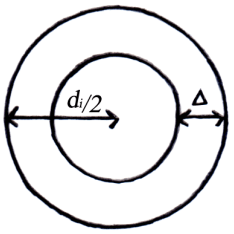
Where

The resistivity of copper $\rho_{cu} = 1.724 \cdot 10^{-9}$ Ωm at 25°C and $2.3 \cdot 10^{-9}$ Ωm at 100°C

The cross sectional area of the copper wire $A_{cu} = \pi \, d_i / 4$

8.3.8 Ac- copper loss

The resistance of the copper wire rises with frequency because of the phenomenas called skin depth and proximity effect. The skin depth is illustrated in the figure below.



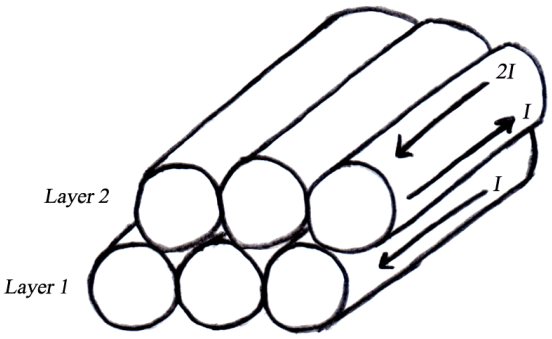
The skin depth Δ, is the distance from the surface of the conductor where current can flow.

$$\Delta = \sqrt{\frac{\rho}{\pi \mu_0 f}}$$

The cross section area of the copper wire in which the current can flow is at AC reduced to

$$A_{cu,AC} = \pi (d_i \cdot \Delta - \Delta^2)$$

The proximity effect is generated when the copperwire is placed in several layers around the core. In the first layer the current I flows and in the second layer the total current will also be I because they are coupled in series. Lenz's law states that the current I flowing in the first layer will induce a current I flowing in the opposite direction in the second layer. Because the total current in the second layer is I there must flow a current of 2I in the upper part of the wire in layer two. The same effect repeats up through the number of layers producing higher and higher current flow.



To find the ac resistance of the wire Jongsma`s model can be used. It states that the ac resistance is the dc resistance times a corrections factor F_R. This factor can be found by the following equation.

$$F_R = \frac{m \cdot \left[M \cdot \left(p \cdot s + \frac{m^2 - 1}{3} \right) \cdot G \right] + s \cdot M_{05}}{p}$$

Where

$$M = \frac{\sinh(2j) + \sin(2j)}{\cosh(2j) - \cos(2j)}$$

$$M_{05} = \frac{j}{2} \cdot \frac{\sinh(j) + \sin(j)}{\cosh(j) - \cos(j)}$$

$$G = 2j \cdot \frac{\sinh(j) - \sin(j)}{\cosh(j) + \cos(j)}$$

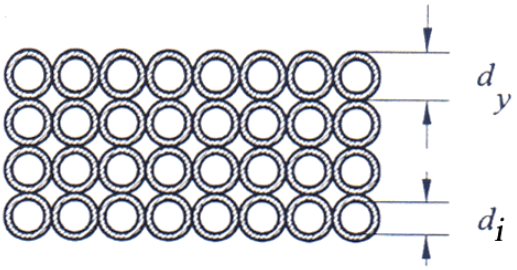
p is the number of layers, m is the integer of p and s = p – m

The parameter φ is defined as

$$j = \frac{d_i \cdot \sqrt{\frac{p}{4}}}{\Delta} \cdot \sqrt{F_C}$$

d_i is the diameter of the copperwire, Δ is the skin depth and F_C is the copper fill factor.

Because the coil is wound with a round insulated wire the copper will not fill out the entire available winding space A_v. this is shown in the figure below



The copper fillfactor can be calculated as

$$F_C = \frac{A_{copper}}{A_v} = \frac{N \cdot p \cdot d_i^2/4}{N \cdot d_y^2} = \frac{p \cdot d_i^2/4}{d_y^2}$$

Now the ac resistance can be calculated as

$$R_{wire,ac} = F_R \cdot R_{wire}$$

The ac-component I_{ac} gives an ac power loss in the copper wire with the resistance $R_{wire,ac}$ determined by

$$P_{cu,ac} = I_{ac}^2 \cdot R_{wire,ac} = I_{ac}^2 \cdot F_R \cdot R_{wire}$$

8.3.9 Total Losses in the Inductor

The total losses in the inductor can be found as

$$P_{dissipated,inductor} = P_{core} + P_{cu,dc} + P_{cu,ac}$$

Notice that when using coupled inductors $P_{cu,dc}$ and $P_{cu,ac}$ has to calculated for each inductor.

8.3.10 Core Temperature

The temperature increase $T_{increase}$ of the inductor is determined by the power dissipated in the coil, $P_{dissipated}$, times the thermal resistance, $R_{th,\ inductor}$, of the inductor. In space where vacuum exist, the heat dissipated in the inductor can only be transferred by heat conduction and heat radiation and not by heat convection so it is difficult to find the thermal resistance but it can be calculated.

The temperature of the inductor is:

$$T_{inductor} = T_{ambient} + T_{increase} = T_{ambient} + R_{th,inductor} \cdot P_{dissipated}$$

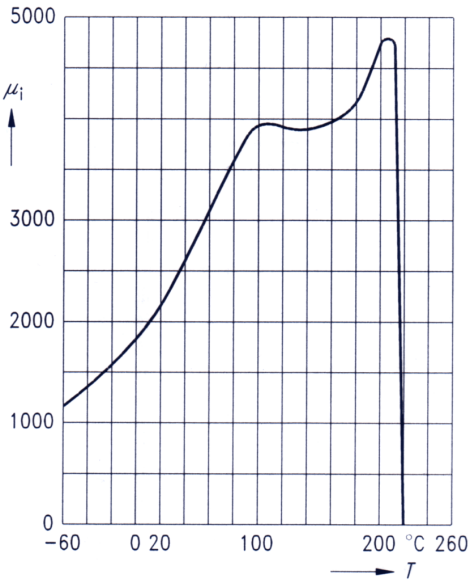
where $T_{ambient}$ is the surrounding temperature.

It is assumed that the heat conduction between the core and the copper windings is so good that they will have the temperature $T_{inductor} = T_{core} = T_{copper}$.

The figure to the right shows the initial permeability μ_i of the core material N87 versus temperature and it can be seen that if the core temperature T_{core} exceeds the core curie temperature at T = 200°C the permeability of the core will decrease to zero. This means the core has lost its ferromagnetic properties and the inductor will no longer be able to store the energy needed because the inductance is proportional to the permeability of the core.

The temperature that will cause the insulation lacquer of the copper wire to melt and cause a short cut in the coil is normally lower the core curie temperature.

As a rule of thumb the temperature of the inductor must never exceed T = 100°C.



8.3.11 RM-cores from Epcos

The following table has been copied from the datasheet. The cores are ungapped:

	RM6-core N87 B65807-J-R87	RM5-core N87 B65805-J-R87	RM4-core N87 B65803-J-R87	
A	36.6	23.8	13	mm^2
A_{min}	31	18	11.3	mm^2
$\mu_{r,core}$	1490	1470	1480	
l_j	28.6	22.1	22	mm
Mass	5.3	3.0	1.65	g
Volume	1050	526	286	mm^3

	RM6-coilformer B65808-N10004-D1	RM5-coilformer B65806-K1004-D1	RM4-coilformer B65804-K1005-D1	
Pins	4	4	5	
b	6.3	5	5.9	mm
h	2.45	1.9	1.3	mm
A_v	15.44	9.5	7.7	mm^2

We have to make an inductor with the inductance L = 100 µH and in the table below the number of turns N needed with respect to different airgabs can be seen.

d_g mm	δ mm	RM6-core N87 B65807-J-R87	RM5-core N87 B65805-J-R87	RM4-core N87 B65803-J-R87
0.10	0.20	N = 22	N = 27	N = 37
0.15	0.30	N = 27	N = 33	N = 44
0.20	0.40	N = 31	N = 38	N = 51

For the coupled inductor the largest diameter of the copper wire can be seen in the tables below.

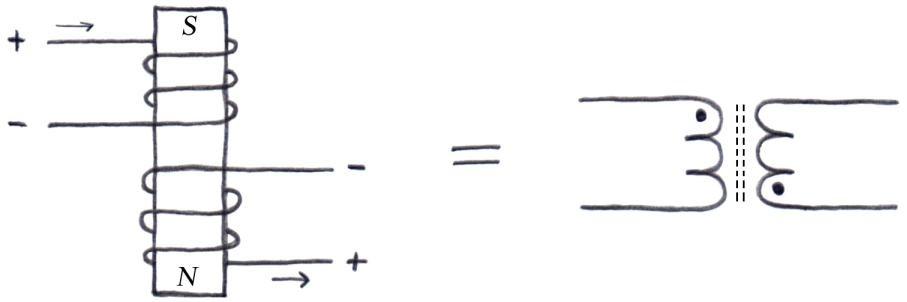
		RM6-coilformer B65808-N10004-D1	
N=	$d_{y,\ max}$	0.54	mm

		RM6-coilformer B65808-N10004-D1
d_i = 0.30 d_y = 0.35 mm	n_{turns}	17
	$n_{layers,max}$	7
	$N_{layers,needed}$	4

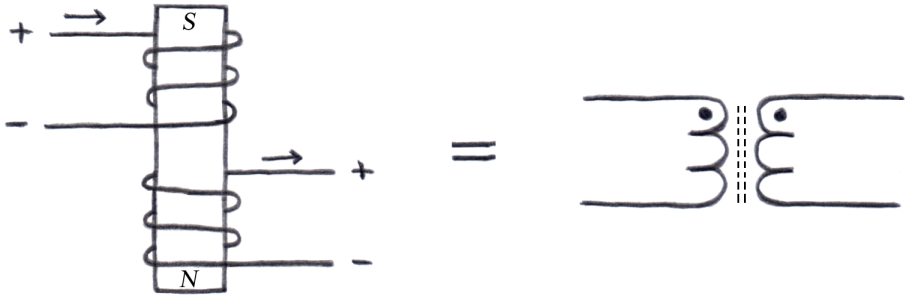
8.3.12 Winding the Coupled Inductor

The coupled inductor must have the right polarity otherwise the DC/DC converter won't work at all. The right hand rule is used to determine the polarity of the inductor. Place the fingers of the right hand in the direction of the current and the North Pole will be in the thumb's direction.

When the first inductor is wound the second inductor can be wound in two different ways as shown in the figure below. The first inductor is the upper one in both cases.



Case A, the second inductor wound in one way



Case B, the second inductor wound in another way

By winding the second inductor either as in case A or B the polarity of the second inductor will changed as show in the figure. The dot represents the positive inductor terminal.
Our coupled inductor must have the polarity as the one shown in case B.

8.4 Controller

There are only a very limited number of flyback and/or SEPIC controllers available. At the time we were going to choose a controller for our design only the Texas TPS43000 controller was available. Some stepup/down controllers were available too, but those were based on a switchmode stepup controller followed by a linear regulator. This configuration is not found to provide a sufficient high efficiency for our purpose.

The Texas TPS43000 controller is a complex controller that supports Buck, Boost, Flyback, and SEPIC configurations. This results in a very flexible controller that can be used in a variety of circuits. Unfortunately this also implies that the controller is rather complex which is an unpleasant feature for our purpose - mainly because there is a higher risk of problems due to radiation.

The controller itself requires some decoupling of 3 pins (V_{In}, V_{Out}, and V_P) - 470 nF each is fine. Two resistors are connected to the drain of the N- and P-FETs. These senses overcurrent conditions (N-MOS), and detects I_{Zero} pulses (P-MOS). A Schottky clamp diode is also required for SEPIC configurations. Also it requires a feedback network that is designed in the next section. Finally a resistor sets the operating frequency:

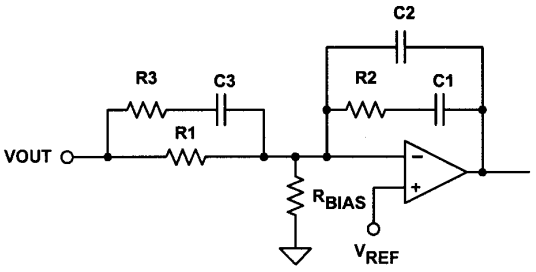
$$R_T = \frac{38000}{f_{SW}} = \frac{38 \cdot 10^9}{100\text{kHz}} = 380\text{k}\Omega \approx 390\text{k}\Omega$$

resulting in a frequency of: $f_{SW} = \frac{38 \cdot 10^9}{390\text{k}\Omega} = 97{,}4\text{kHz}$.

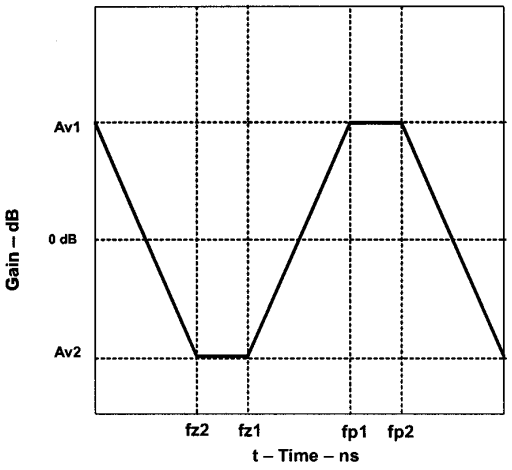
Even though the controller can operate at up to 2 MHz, we decided to operate it at only 100 kHz. This is mainly because we wanted to reduce the problems of highspeed switching circuits to begin with, and because core losses are increasing rapidly at frequencies above 100 kHz.

8.5 Feedback

The TPS43000 uses an error amplifier compensation network as depicted in the figure below. The gain response is shown in the same figure.



Type III Error Amplifier Compensation Network



Type III Error Amplifier Compensation Gain Response

The goal of this design is to set the crossover frequency above the resonant frequency of the LC filter (this prevents filter oscillations during a transient response), but below the lowest right half-plane zero. This is accomplished by setting the two zeros ($f_{z1} = \frac{1}{2\pi \cdot R_2 \cdot C_1}$, and $f_{z2} \approx \frac{1}{2\pi \cdot R_1 \cdot C_3}$, assuming $R_1 >> R_3$) in the compensation network before the LC double pole frequency, finally the two poles ($f_{p1} = \frac{1}{2\pi \cdot R_3 \cdot C_3}$, and $f_{p2} \approx \frac{1}{2\pi \cdot R_2 \cdot C_2}$, assuming $C_1 >> C_2$) should be placed respectively to cancel the ESR zero of the output capacitor, and one-half decade above the crossover frequency. Let's repeat the data we need for these calculations:

$V_{in,\,min}$	2,6 V
$V_{in,\,max}$	6,2 V
V_{out}	3,6V
C_{out}	220 uF
R_{Cout}	100 mΩ
L	100 uH
V_{Ref}	0,8 V

First, we must determine the LC pole frequency, this is dependent of the duty cycles, which can be estimated to: $D = \frac{V_{out}}{V_{in} + V_{out}} = \frac{3{,}6V}{V_{in} + 3{,}6V}$, resulting in:

$$D_{min} = \frac{V_{out}}{V_{in} + V_{out}} = \frac{3{,}6V}{2{,}6V + 3{,}6V} = 0{,}5806, \text{ and } D_{max} = \frac{V_{out}}{V_{in} + V_{out}} = \frac{3{,}6V}{6{,}2V + 3{,}6V} = 0{,}3673,$$

the average dutycycle is thus: (0,5806+0,3673) / 2 = 0,4740.

$$f_{LC} = \frac{1 - D}{2\pi\sqrt{LC}} = \frac{1 - 0{,}4740}{2\pi\sqrt{100\mu H \cdot 220\mu F}} = 565Hz$$

Texas recommend to set the crossover frequency a decade above f_{LC}, that is at 5700 Hz.

Next we must set the output voltage by the voltage divider formed by R_1 and R_{BIAS}. Choosing R1 = 160 kΩ we get: $R_{BIAS} = \frac{R_1 \cdot \frac{V_{ref}}{3{,}6V}}{1 - \frac{V_{ref}}{3{,}6V}} = 45{,}7\ k\Omega \approx 47\ k\Omega$. This results in an output voltage of: $V_{Out} = V_{Ref} \frac{R_1 + R_{BIAS}}{R_{BIAS}} = 0{,}8\frac{160 + 47}{47} V = 3{,}52\ V$.

First f_{z2} is set to 200 Hz: $f_{z2} = \frac{1}{2\pi \cdot 160k \cdot C_3} = 200\ Hz$ => C_3 = 5 nF ≈ 4,7 nF, resulting in f_{z2} = 212 Hz. Next f_{z1} is set to 300 Hz (R_2 is chosen as 24 kΩ):

$f_{z3} = \frac{1}{2\pi \cdot 24k \cdot C_1} = 300\ Hz$ => C_1 = 22,1 nF ≈ 22 nF, resulting in f_{z1} = 301 Hz.

The first pole is set to cancel the ESR zero of the output capacitor: $f_{ESR} = \frac{1}{2\pi \cdot R_{ESR} \cdot C} = \frac{1}{2\pi \cdot 0{,}1\Omega \cdot 220\mu F} = 7234\ Hz$. $f_{p1} = \frac{1}{2\pi \cdot R_3 \cdot 4{,}7nF} = 7234Hz$ => R_3 = 4,69 kΩ ≈ 4,7 kΩ, resulting in f_{p1} = 7205 Hz. Finally $f_{p2} = \frac{1}{2\pi \cdot 24k\Omega \cdot C_2} = 30143Hz$ => C_2 = 224 pF ≈ 220 pF, resulting in f_{p2} = 30143 Hz

We'll summarize the results here (mid column is the component number in the Protel Schematic file):

f_{z1}	301 Hz
f_{z2}	212 Hz
f_{p1}	7205 Hz
f_{p2}	30140 Hz

R_1	R_{23}	160 kΩ
R_2	R_{21}	24 kΩ
R_3	R_{24}	4,7 kΩ
R_{BIAS}	R_{22}	47 kΩ

C_1	C_6	22 nF
C_2	C_2	220 pF
C_3	C_7	4,7 nF

8.6 Linear 3,3V Converter

We need a low-dropout linear controller. For this purpose we've selected the REG103 from Texas instruments. It is available in a fixed 3,3V version. Typical dropout voltage at 500 mA is 115 mV. It features fast transient response, low noise, and high accuracy. Also it has a foldback current limiter (700 mA) and thermal protection.

The device requires an input capacitor of only 100 nF, while the output capacitor is optional. We expect to use one in the final design, however.

9. Tests

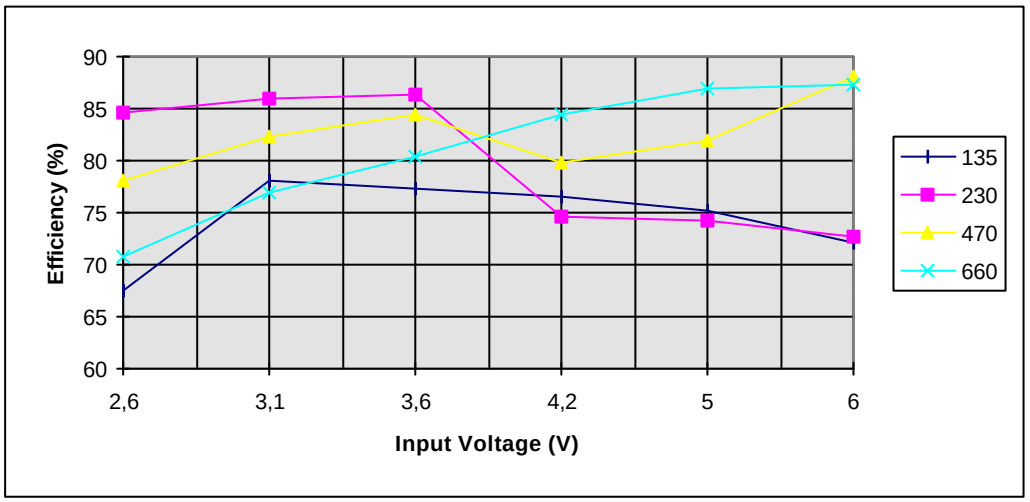
9.1 Test of Housekeeping System

The power subsystem was connected to the ISA Data Acquisition Card we developed during the previous project. It is interesting to note that the ISA subsystem is operating at 5V logic, and that the power subsystem is operating at 3,3V logic. Fortunately the max1281 ADC operates with up to 6V on the digital inputs, and the input/output levels of the two systems are matched too. It is therefore possible to connect the 3,3V power subsystem directly to the ISA Data Acquisition Card, although an adapter is needed for the wiring.

The test software can be seen in Appendix K. We used the program to sample all the data points, and by what we found that everything worked fine. The noise was found to be within 2 mV / 1 mA. This is actually the best accuracy a 12 bit ADC can deliver. The deviation from voltages / currents was within the limits of accuracy of the resistors. As mentioned earlier it is necessary to account for these inaccuracies by means of software.

9.2 Efficiency Tests of the DC/DC Converter

We did an efficiency test of the DC/DC converter. The results can be seen in the figure:



10. Future Work

A. Design:

- We need to select the flightpin and killswitches
- Global shutoff on latchup conditions
- Current limiter for the battery charger

B. Testing:

- The power supply unit, along with the other subsystems, must be exposed to high energy particles so it can be seen if the latch up protection circuitry works.
- Simulations with a satellite model that has body mounted solar cells will be done in order to simulate the satellite in orbit.

11. Conclusion

This part of the project was more like a traditional project at DTU. This time we had the specifications, most of the interfaces etc. We then went on designing the different part of the systems, and finally we tested them.

One of the most interesting results of the project is that the Li-Ion Polymer packaging is useless under space conditions, because the battery lost almost all of the capacity. Also we realized that the Panasonic CGR18650H battery works fine in space.

Wether we're going to use the battery heating system or not depends on the orbit we're going to be put into. Even though the battery heating system may not be a necessity even at -20 °C it will allow us to draw additional energy from the battery.

We have build a DC/DC converter based on the Sepic topology. The converter works, but it needs to be optimized, both according to losses, and output noise.

12. References and Literature

12.1 References

[Cheng] David K. Cheng: Fundamentals of Engineering Electromagnetics, Addison-Wesley, 1992, ISBN 0201566117

12.2 Links to Websites

[ST02] http://www.stensat.org/Docs/liion_test.html

[TU02] http://www.css.tayloru.edu/~physics/picosat/news/paper/SmallSat%20Taylor%206-27-01.pdf

12.3 Secondary Literature

Batteries:
David Linden: Handbook of batteries, 2nd edition
Mcgraw-Hill Book Company Inc., 1995

DC/DC Converters:
Michael A.E. Andersen, Arne Hansen, Henrik Havemann, and Jørgen Kaas Pedersen:
Grundlæggende effektelektronik, DTU, 1997

Mohan, Undeland, and Robbins:
Power Electronics, Converters, Applications and Design, 2nd Edition, Wiley, 1995

Robert W. Erickson, and Dragon Maksimovic:
Fundamentals of Power Electronics, 2nd edition, Kluwer Academic Publishers, 1999

Sepic:
Maxim:
SEPIC Equations and Component Ratings, April 2002
http://www.maxim-ic.com/tarticle/view_article.cfm/article_id/1051

Lauren Liu and Hanns Chiu:
The Power Management of PDA - The Application of SEPIC Circuit, AIC, April 2001
http://www.metatech.com.hk/appnote/aic/pdf/AN01-SW01EN.pdf

Undervoltage Protection:
Albert Lee:
Li-Ion Battery Protection Circuit Draws Only 4.5 uA, Electronic Design, December 1999
http://www.elecdesign.com/1999/dec0699/ifd/3IFD.pdf

12.4 Datasheets

Analog:

ADP3820 http://www.analog.com/productSelection/pdf/ADP3820_a.pdf

Fairchild:

BAT54 http://www.fairchildsemi.com/ds/BA/BAT54.pdf

Epcos:

RMx http://www.eastern-components.com/epcos-elib.html

Linear:

LT1389 http://www.linear.com/pdf/1389fa.pdf

LT1494 http://www.linear.com/pdf/149456fb.pdf

Maxim:

Max472 http://dbserv.maxim-ic.com/quick_view2.cfm?qv_pk=1108

Max4172 http://pdfserv.maxim-ic.com/arpdf/MAX4172.pdf

Max890L http://dbserv.maxim-ic.com/quick_view2.cfm?qv_pk=1526

Max1281 http://pdfserv.maxim-ic.com/arpdf/MAX1280-MAX1281.pdf

Max1879 http://dbserv.maxim-ic.com/quick_view2.cfm?qv_pk=2544

Murata:

20uF, 10V Part Number: GJ232NF51A226ZD01L
http://search.murata.co.jp/Ceramy/owa/CATALOG.showcatalog?sHinnmTmp=GRM235Y5V226Z10&sLang=2&sNhnm=GJ232NF51A226ZD01L&sHnTyp=NEW

Philips:

PRLL5817 http://www.semiconductors.philips.com/acrobat/datasheets/PRLL5817_18_19_2.pdf

Texas:

BQ24200 http://www-s.ti.com/sc/ds/bq24200.pdf

TPS43000 http://www-s.ti.com/sc/ds/tps43000.pdf

Vishay:

Si9803DY http://www.vishay.com/document/70638/70638.pdf

Si9804DY http://www.vishay.com/document/70626/70626.pdf

Zetex:

ZHCS1000 http://www.zetex.com/3.0/pdf/ZHCS1000.pdf

Appendix A - Power Budget

1 page

Detumbling Power Budget Prior to Radiation

		U (V)	I (mA)	dutycycle	Average power (mW)	P when NOT transmitting (mW)	P when transmitting (mW)	3V3 (Max) (mA)	Unreg, total,max (mA)	Notes
Attitude	**Magnetorquers**	3,3 - 8	<= 50	0,99	150	150	150	0	50	
	Magnetometer 1	3,3	<= 50	0,01	3	3	3	50	50	
	Magnetometer 2	3,3	2	1	7	7	7	2	2	
	Sunsensor	3,3	8	0,02	1	1	1	8	8	
OBC	**Normal operation**	3,3	50	1	165	165	165	50	50	
	Bootup	3,3	110	0,0006	0,2017	0,2017	0	110	110	
	Upload	3,3	110	0,0069	2,5	0	0	0	0	1)
Radio	**Beacon**	3,3	2	1	6,6	6,6	6,6	2	2	
	Receiver	3,3	20	1	66	66	66	20	20	
	Transmitter	3,3	20	0,0833	5,5	0	66	20	20	
	PA	3,0 - 6,1	270	0,0833	83,25	0	1000	0	270	
Camera		3,3	75	0,0556	14	14	0	65	0	2) 3)
Thether	**Normal**	3,3	20	1	66	66	66	0	0	4)
	Peak	3,3	100	0	0	0	0	0	0	4)
Total					570,1	478,8	1530,6	327	582	
								/\		

Bootup/Upload doesn't occur at the same time
Camera doesn't run at bootup, but possibly at the same time as the tether
Camera doesn't run at the same time as the transmitter
Tether doesn't run at bootup/upload => tether = 0mA

Appendix B - Weight Budget

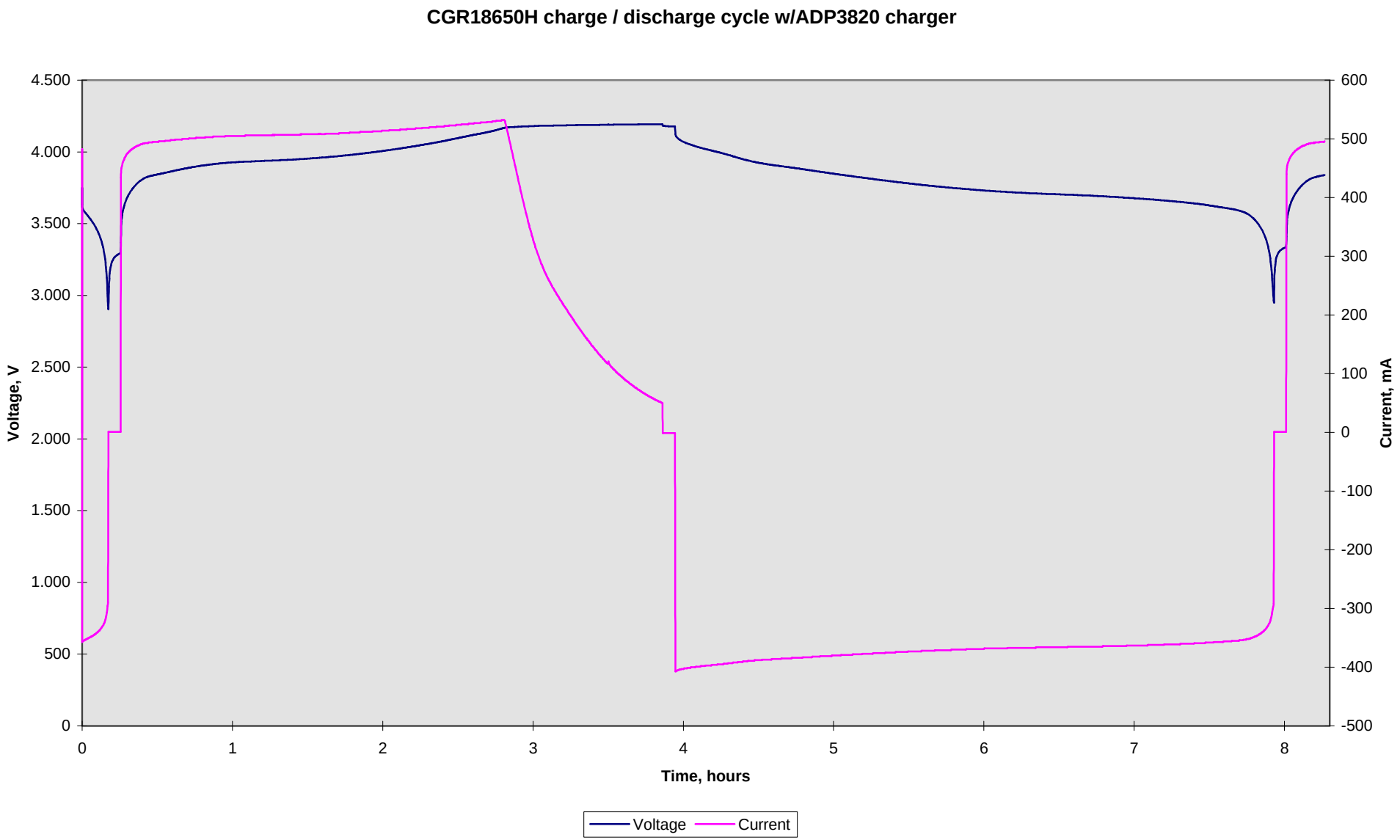
1 page

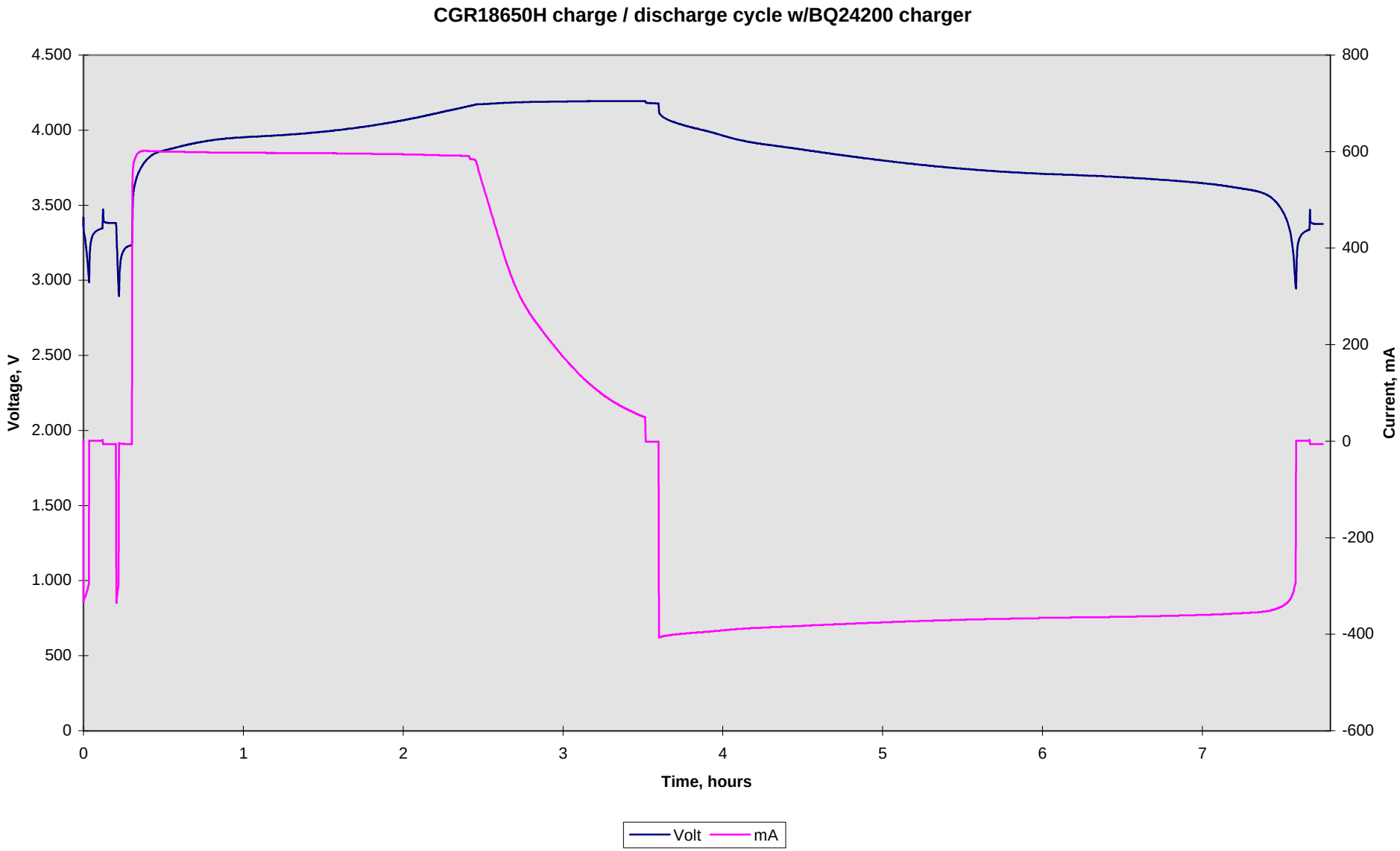
DTUsat vægtbudget pr. 24/04/2002

		VÆGT				
System		**Min**	**Max**	**Sandsynlig**	**Spredning**	**Bemærkninger**
Struktur, (kasse;-)						
	Paneler	111	150	125	+20% / -11%	AutoCad beregning
	Hjørnestolper	70	120	75	+60% / -7%	AutoCad beregning
	Fjeder til udskydning	3	10	4	+150% / -25%	Vi skal bruge en bestemt fjeder.... Som rent faktisk er ret lille :-)
	Lim/Skruer	10	30	25	+20% / -60%	Gæt
	Holdere til ACDS, PCB, ETC.	50	120	70	+71% / -29%	Ingen decideredе holdere til tether og kamera.
	Samlet:	**244**	**430**	**299**	+44% / -18%	300 g totalt for 1-1,5 mm alu panel
						Opdateret: 24/4-2002
Backplane						Ukendt, da metode endnu ikke er fastlagt
	Ledinger	20	50	40	+25% / -50%	
	Stik	15	50	15	+233% / 0%	
	Etc (Epoxy / div holdere)	20	50	40	+25% / -50%	
	Samlet:	**55**	**150**	**95**	+58% / -42%	
						Opdateret: 24/4-2002
Power, print						
	Printplade	10	15	13	+15% / -23%	
	Komponenter	15	40	25	+60% / -40%	
	Thermisk design	5	9	4	+125% / 25%	
	Samlet:	**30**	**64**	**42**	+52% / -29%	
						Opdateret: 3/4-2002
Power						
	Solpaneler incl. Glasfront	60	100	80	+25% / -25%	Regnet som 6 paneler på 5 sider á 1.5x40x20 i glas
	Killswitche	10	20	10	+100% / 0%	
	Flight pin	5	15	8	+88% / -38%	
	Test plug	5	15	8	+88% / -38%	
	Batterier	40	40	40	+0% / 0%	Panasonic CGR18650H
	Samlet:	**120**	**190**	**146**	+30% / -18%	
						Opdateret: 3/4-2002
OBC, print						
	Printplade	15	20	18	+11% / -17%	
	Komponenter	5	15	10	+50% / -50%	
	Strålingsbeskyttelse	0	30	30	+0% / -100%	2 mm x 40 mm x 40 mm x 2 stk
	Thermisk design	5	9	5	+80% / 0%	
	Samlet:	**25**	**74**	**63**	+17% / -60%	
						Opdateret: 24/4-2002
ACDS, print						
	magnetorquers	40	50	45	+11% / -11%	Bør snarest fastlægges ved et praktisk forsøg, også for at få klarlagt montage
	Solsensorer Print	5	18	8	+125% / -38%	
	Solsensorer Komponenter	8,5	17	8,5	+100% / 0%	
	ACDS Printplade	12	20	16	+25% / -25%	
	ACDS Komponenter	5	10	8	+25% / -38%	
	Thermisk design	12	23	12	+92% / 0%	
	Samlet:	**82,5**	**138**	**97,5**	+42% / -15%	
						Opdateret: 25/2-2002
Radio, print						
	Printplade	10	15	13		
	Komponenter	5	15	10	+50% / -50%	
	Thermisk design	5	9	5	+80% / 0%	
	Samlet:	**20**	**39**	**28**	+39% / -29%	
						Opdateret: 25/2-2002
Antenne						
	Selve antennerne	5	25	15	+67% / -67%	
	Holdere til antenner	4	30	10	+200% / -60%	
	Antenne, fødenetværk	15	50	20	+150% / -25%	
	Mekanisme til frigørelse	10	50	30	+67% / -67%	
	Samlet:	**34**	**155**	**75**	+107% / -55%	
						Opdateret: 24/4-2002
Kamera, incl. holder						
	Elektronik	15	25	20	+25% / -25%	
	Optik mm.	15	25	20	+25% / -25%	
	Holder	15	25	20	+25% / -25%	
	Samlet:	**45**	**75**	**60**	+25% / -25%	
						Opdateret: 24/4-2002
Tether, incl holder						Designvægt er 100g. Dette tilpasses ved at variere i selve tetherens størrelse.
	Tetherholder	10	30	20	+50% / -50%	Jeg har indført forskellige estimater for Min/Max/Forventede masser.
	Tether	25	70	55	+27% / -55%	Vægten af emitter og strømforsyning er ret sikre, mens elektronik ikke er.
	Electronik	10	20	15	+33% / -33%	Jo mindre de andre vægte bliver, jo længere/solidere kan selve tetheren blive.
	Strømforsyning	5	15	5	+200% / 0%	Som worst-case eksemplet viser, så ville det være rart hvis den samlede
	Electronemitter	5	10	5	+100% / 0%	design-vægt kunne være over 100g! Den oprindelige plan for tetheren var
	Samlet:	**55**	**145**	**100**		nøjagtig worst-case eksemplet med 200g total: 135g tether, 65 for alt andet....
Samlet:		**710,5**	**1460**	**1005,5**	+45% / -29%	Opdateret: 25/2-2002
						Ret dine egne tal, nulsæt grænserne ved sikkerhed og skriv dig ind i historien.
						Mangler der et delsystem, så tilføj det - hold dokumentet ved lige og realistisk.
						GEM VENLIGST I EXCEL 95 FORMAT!
						Giv venligst en bemærkning, hvis der er foretaget rimelige beregninger for budet
						History:
				14-01-02		Oprettet af radio med tal fra MEK
				15-01-02		Rettelser fra MEK
				16-01-02		Tilføjelse af Michael Thomsen
				21-01-02		Omskrevet totalt af MEK og overladt til fremtiden ;-)
				21-01-02		Tether beregning udspecificeret, og variationer anført.
				06-02-02		Power opdateret
				25-02-02		ACDS og Tether opdateret.
				03-04-02		Power opdateret
				24-04-02		Opdateret ved interface møde

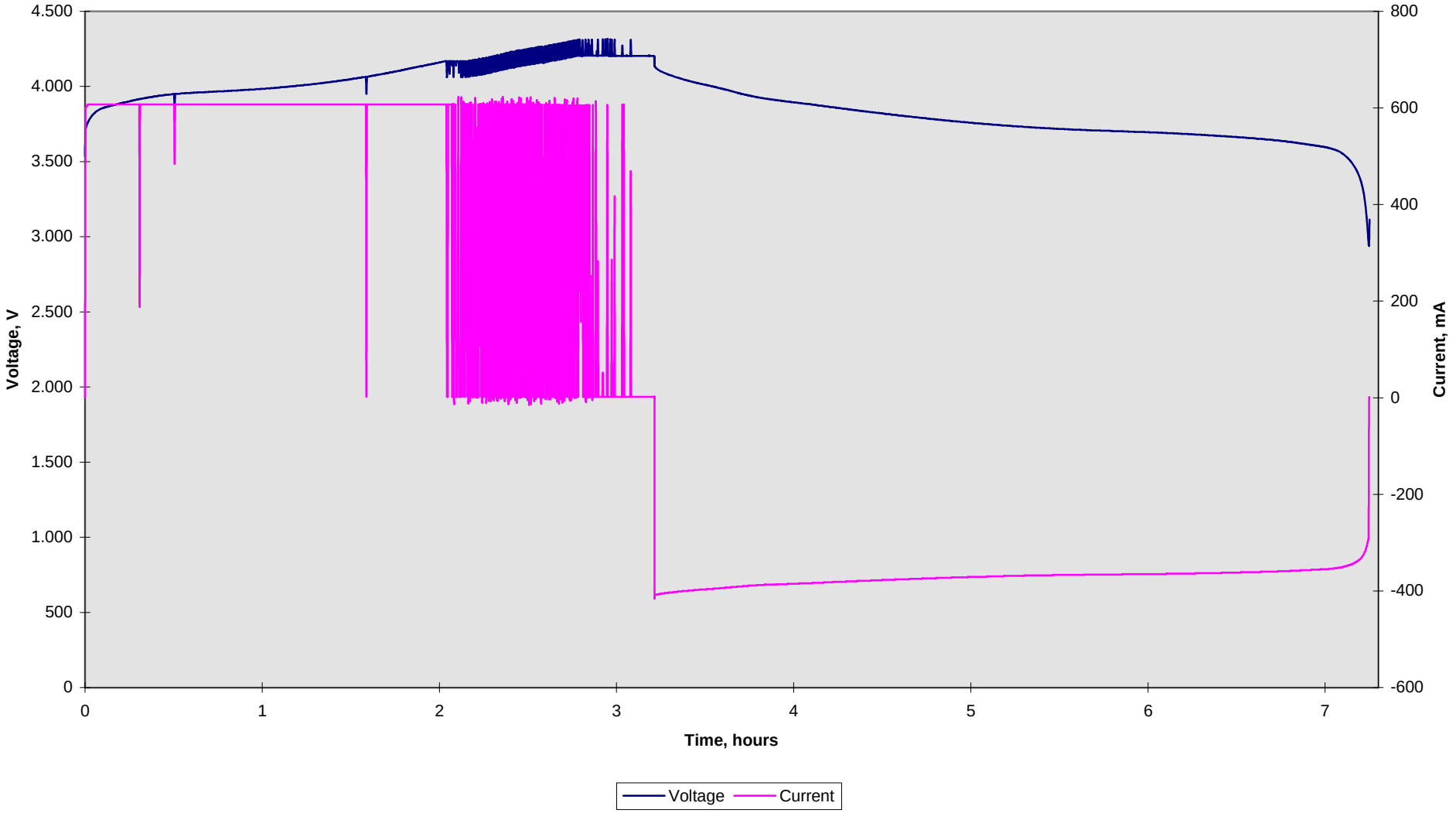
Appendix C - Battery Tests

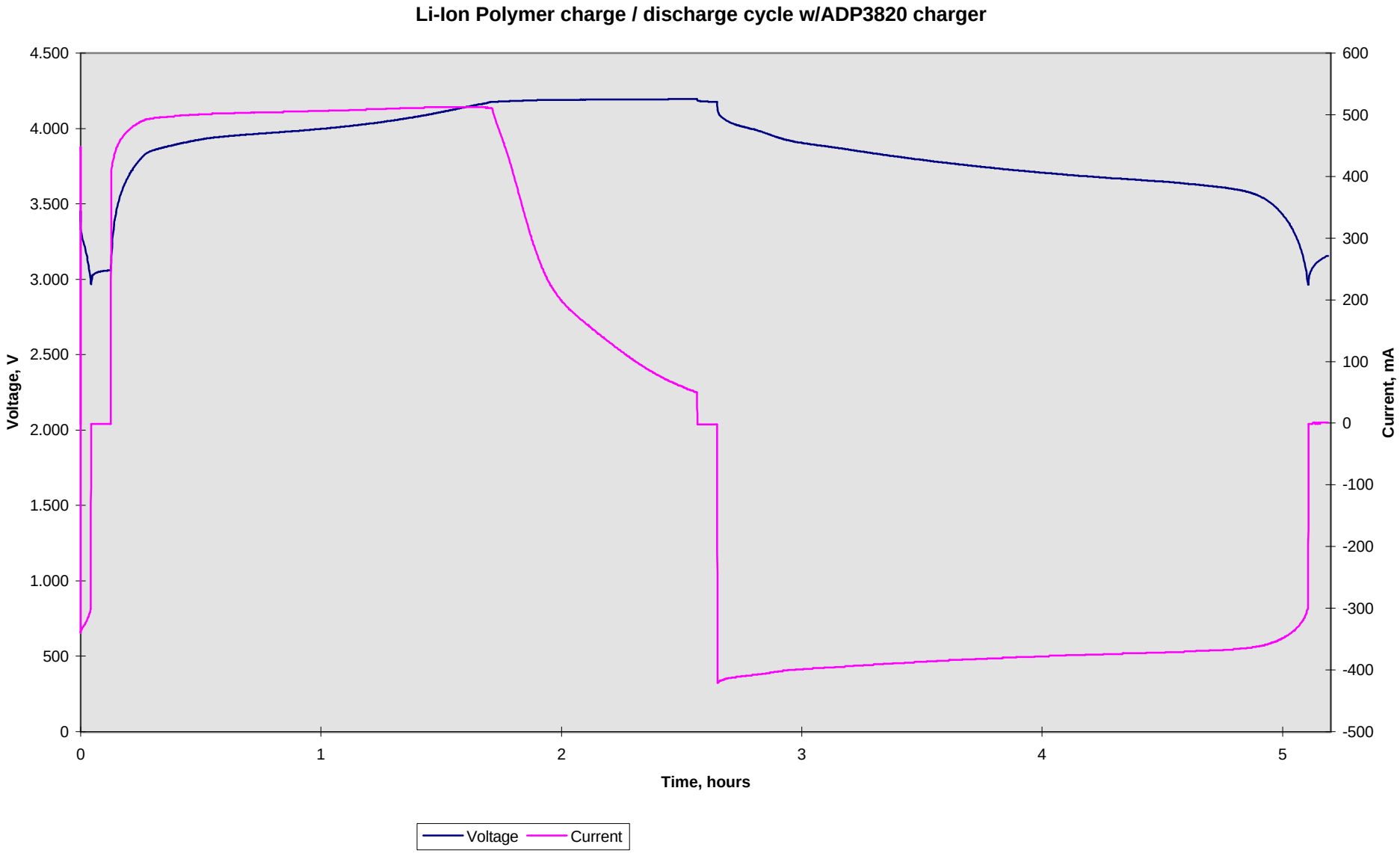
Total 10 pages

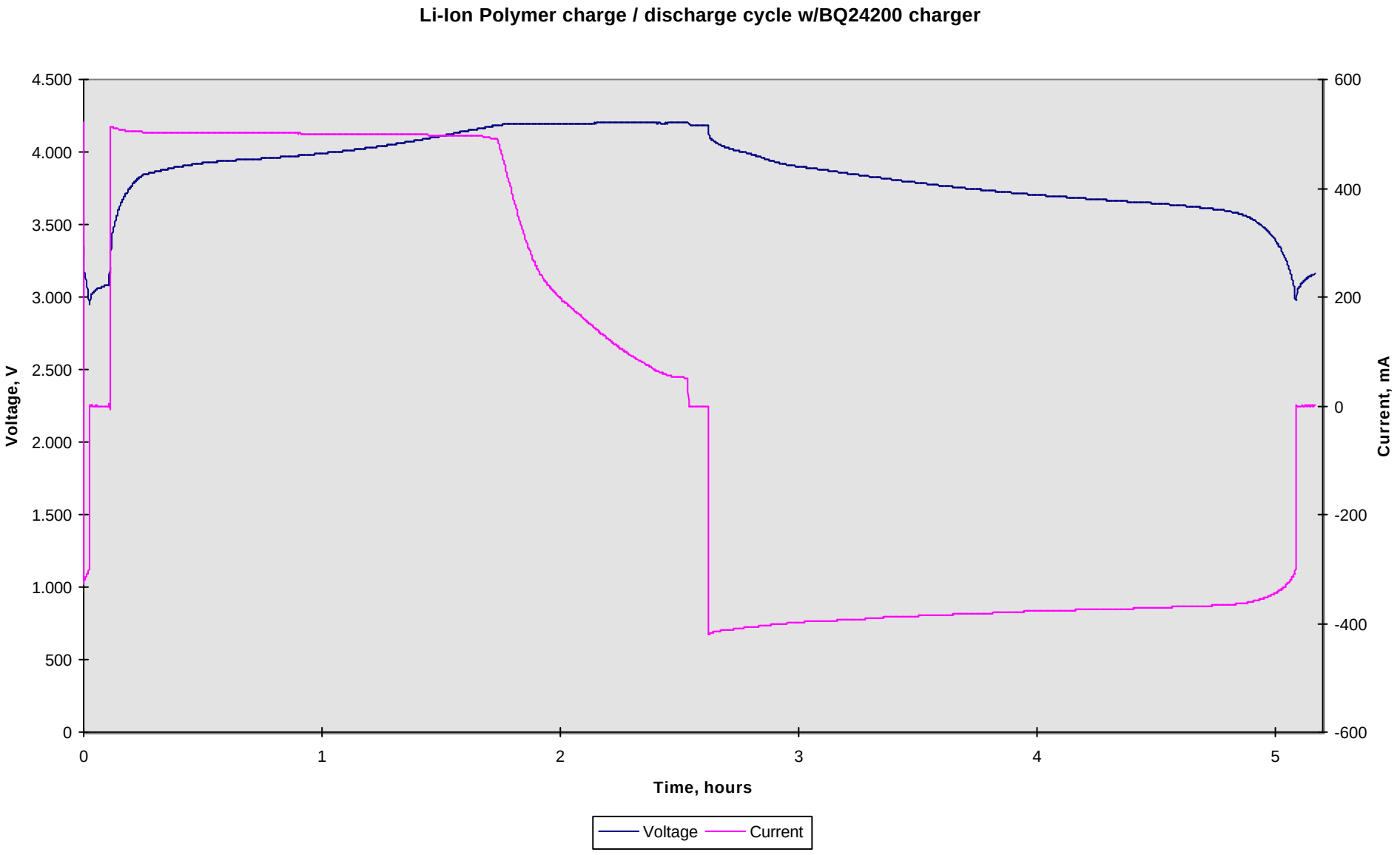

CGR18650H charge / discharge cycle w/ADP3820 charger
Voltage, V
Current, mA
Time, hours
4.500
4.000
3.500
3.000
2.500
2.000
1.500
1.000
500
0
600
500
400
300
200
100
0
-100
-200
-300
-400
-500
0
1
2
3
4
5
6
7
8
Voltage
Current

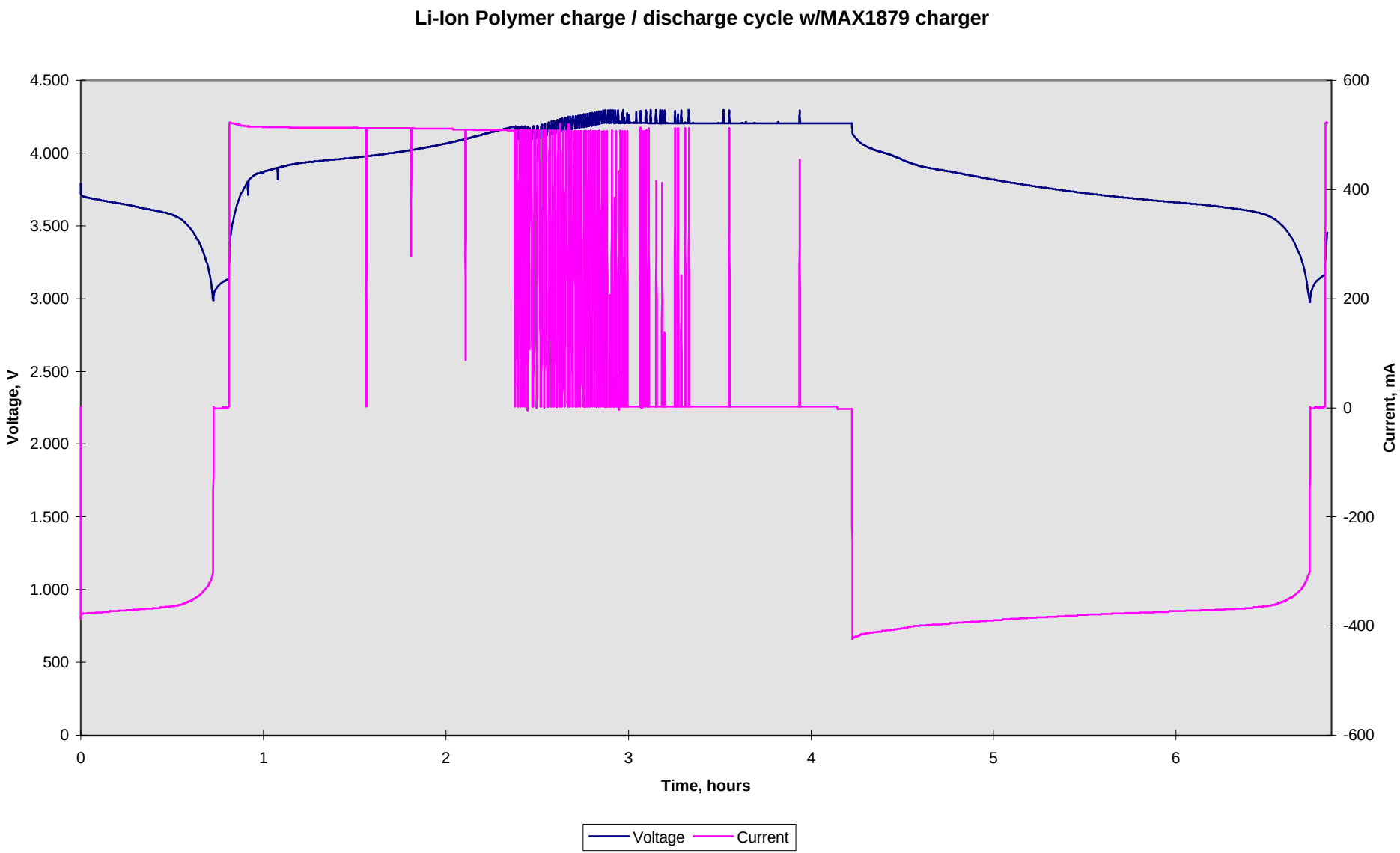

CGR18650H charge / discharge cycle w/BQ24200 charger
Voltage, V
Current, mA
Time, hours
4.500
4.000
3.500
3.000
2.500
2.000
1.500
1.000
500
0
800
600
400
200
0
-200
-400
-600
0
1
2
3
4
5
6
7
Volt
mA

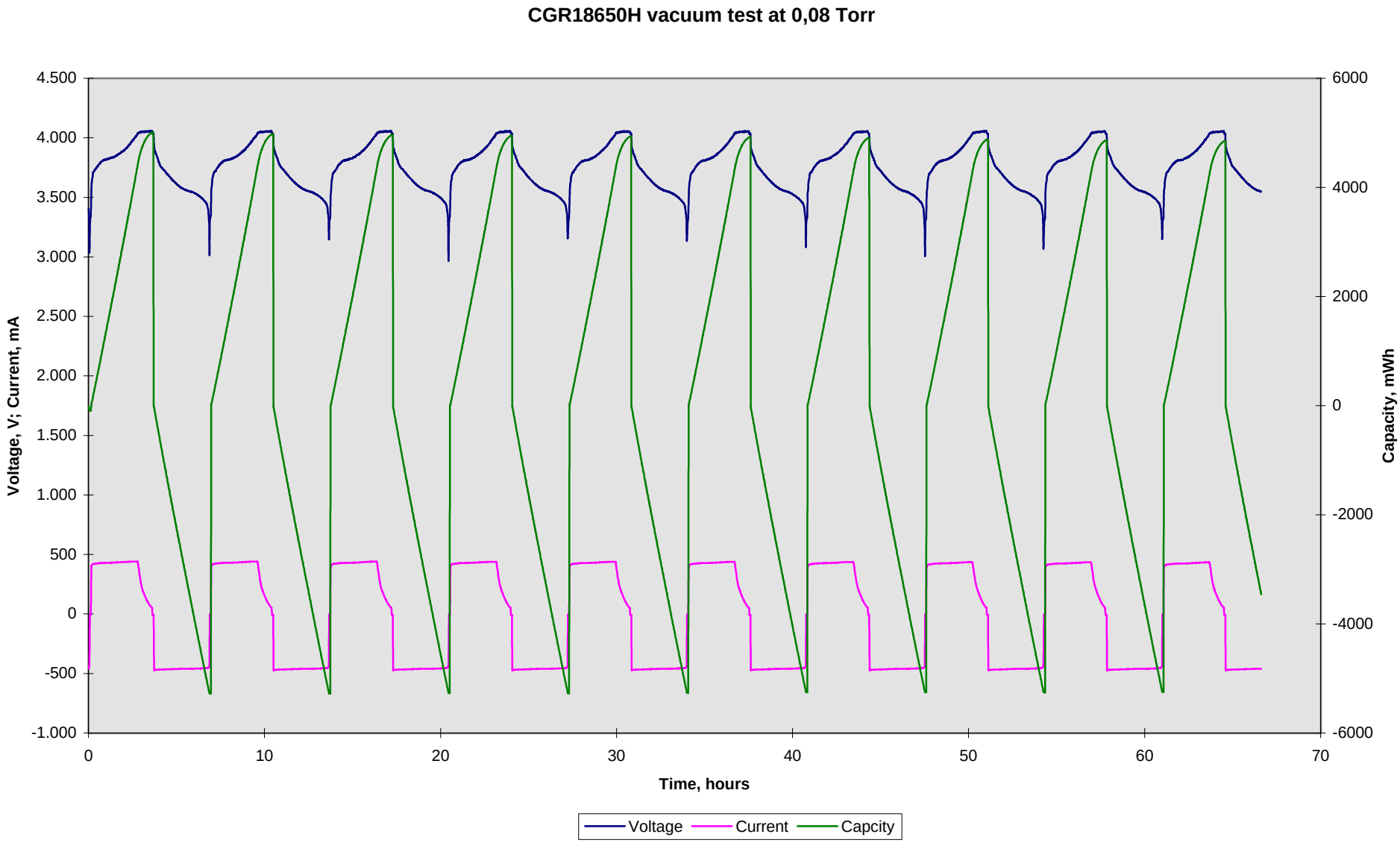
CGR18650H charge / discharge cycle w/max1879 charger

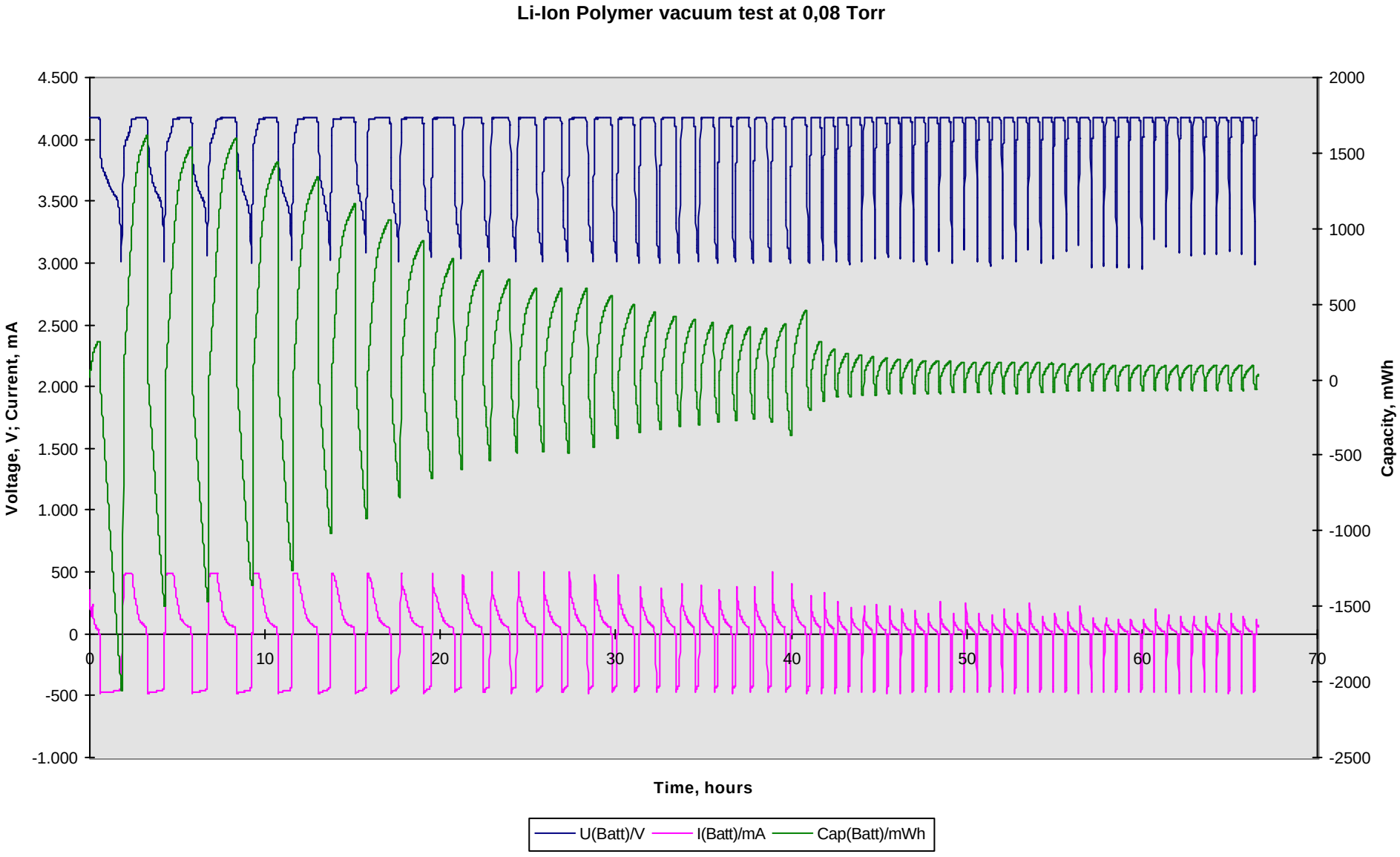


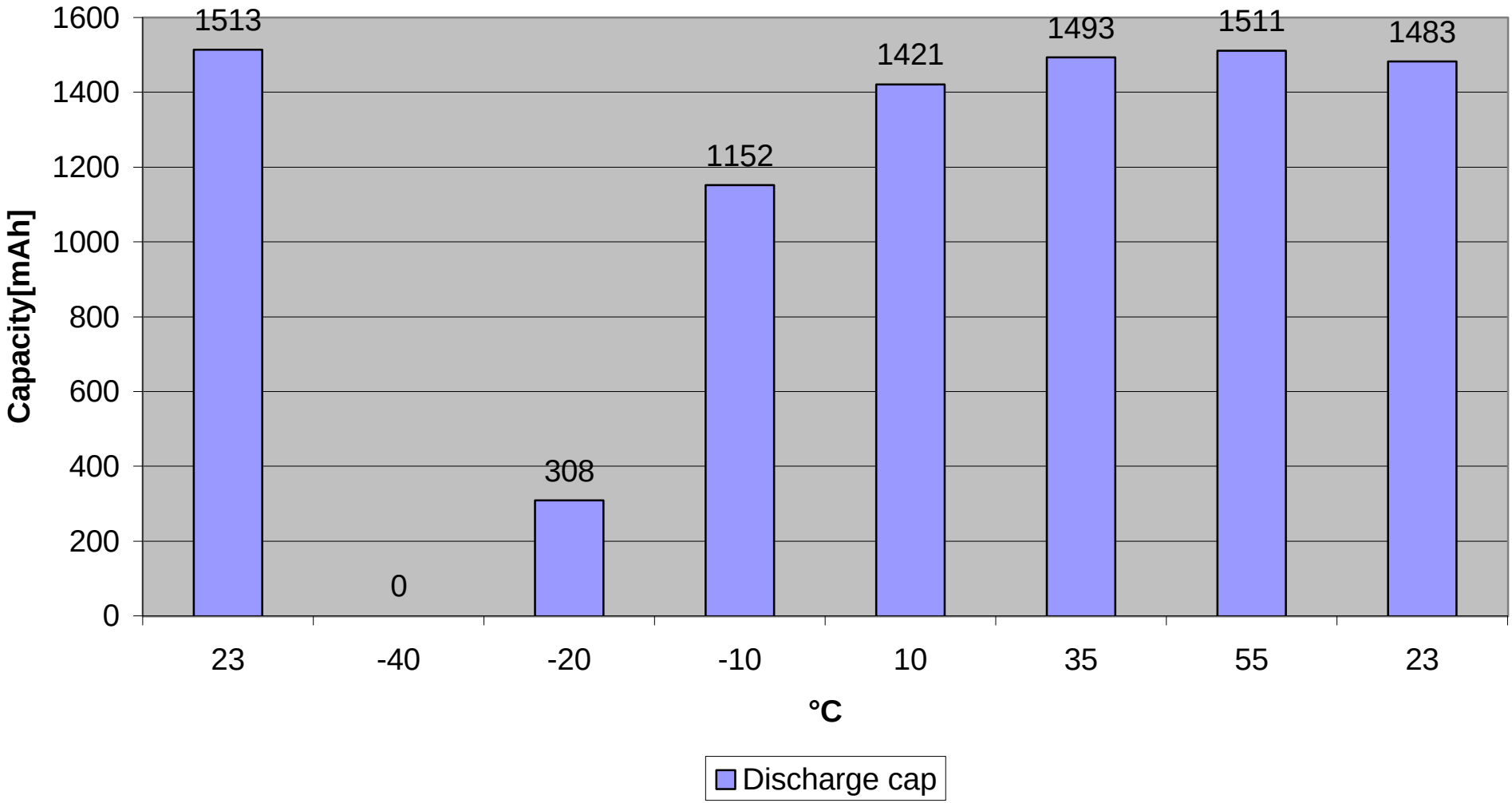

Li-Ion Polymer charge / discharge cycle w/ADP3820 charger
Voltage, V
4.500
4.000
3.500
3.000
2.500
2.000
1.500
1.000
500
0
Current, mA
600
500
400
300
200
100
0
-100
-200
-300
-400
-500
0
1
2
3
4
5
Time, hours
Voltage
Current

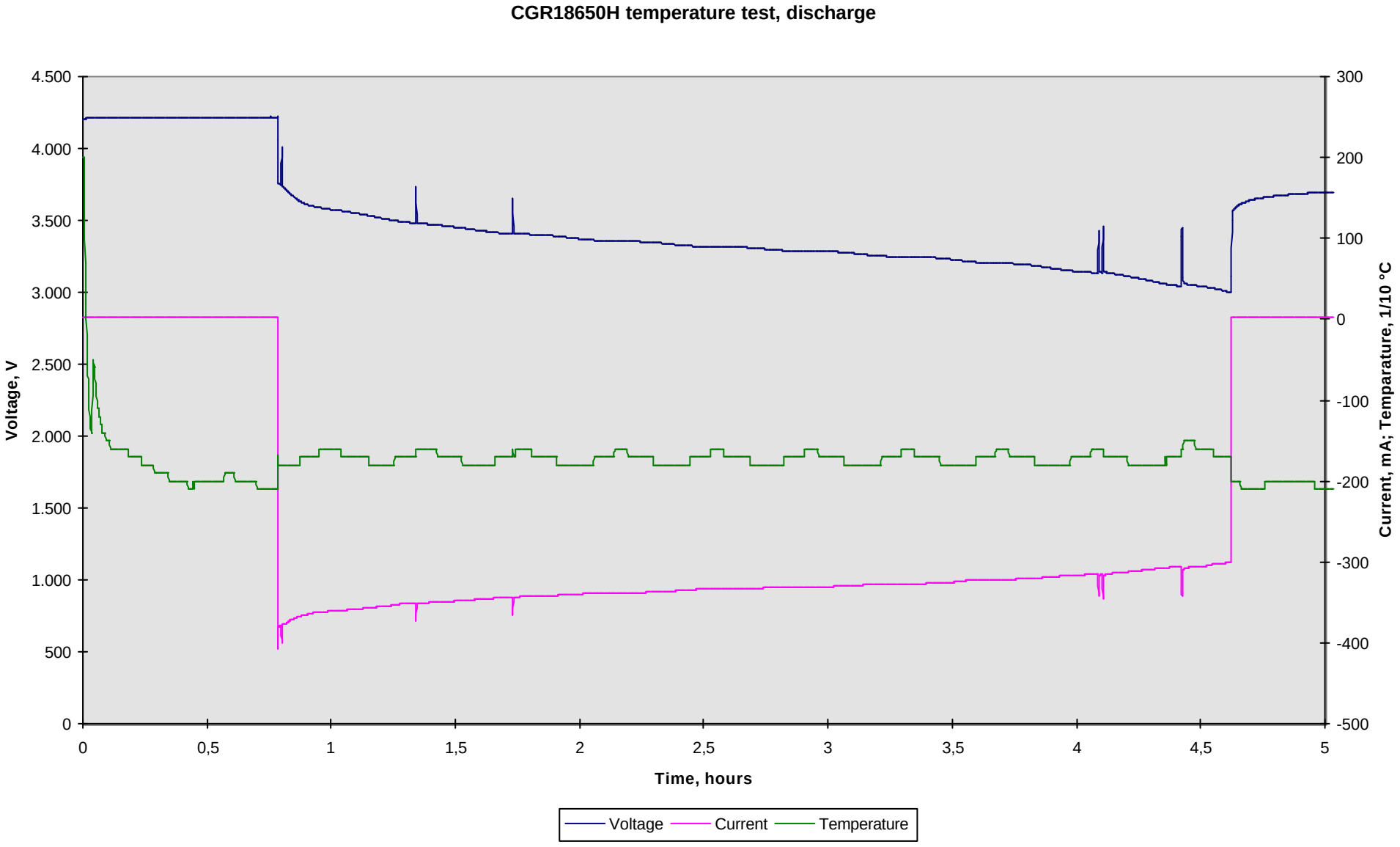

Li-Ion Polymer charge / discharge cycle w/BQ24200 charger
4.500
4.000
3.500
3.000
2.500
2.000
1.500
1.000
500
0
Voltage, V
600
400
200
0
-200
-400
-600
Current, mA
0
1
2
3
4
5
Time, hours
Voltage
Current


Li-Ion Polymer charge / discharge cycle w/MAX1879 charger
Voltage, V
Current, mA
Time, hours
4.500
4.000
3.500
3.000
2.500
2.000
1.500
1.000
500
0
600
400
200
0
-200
-400
-600
0
1
2
3
4
5
6
Voltage
Current


CGR18650H vacuum test at 0,08 Torr
Voltage, V; Current, mA
Capacity, mWh
Time, hours
4.500
4.000
3.500
3.000
2.500
2.000
1.500
1.000
500
0
-500
-1.000
6000
4000
2000
0
-2000
-4000
-6000
0
10
20
30
40
50
60
70
Voltage
Current
Capcity


Li-Ion Polymer vacuum test at 0,08 Torr
Voltage, V; Current, mA
Capacity, mWh
Time, hours
4.500
4.000
3.500
3.000
2.500
2.000
1.500
1.000
500
0
-500
-1.000
2000
1500
1000
500
0
-500
-1000
-1500
-2000
-2500
0
10
20
30
40
50
60
70
U(Batt)/V
I(Batt)/mA
Cap(Batt)/mWh

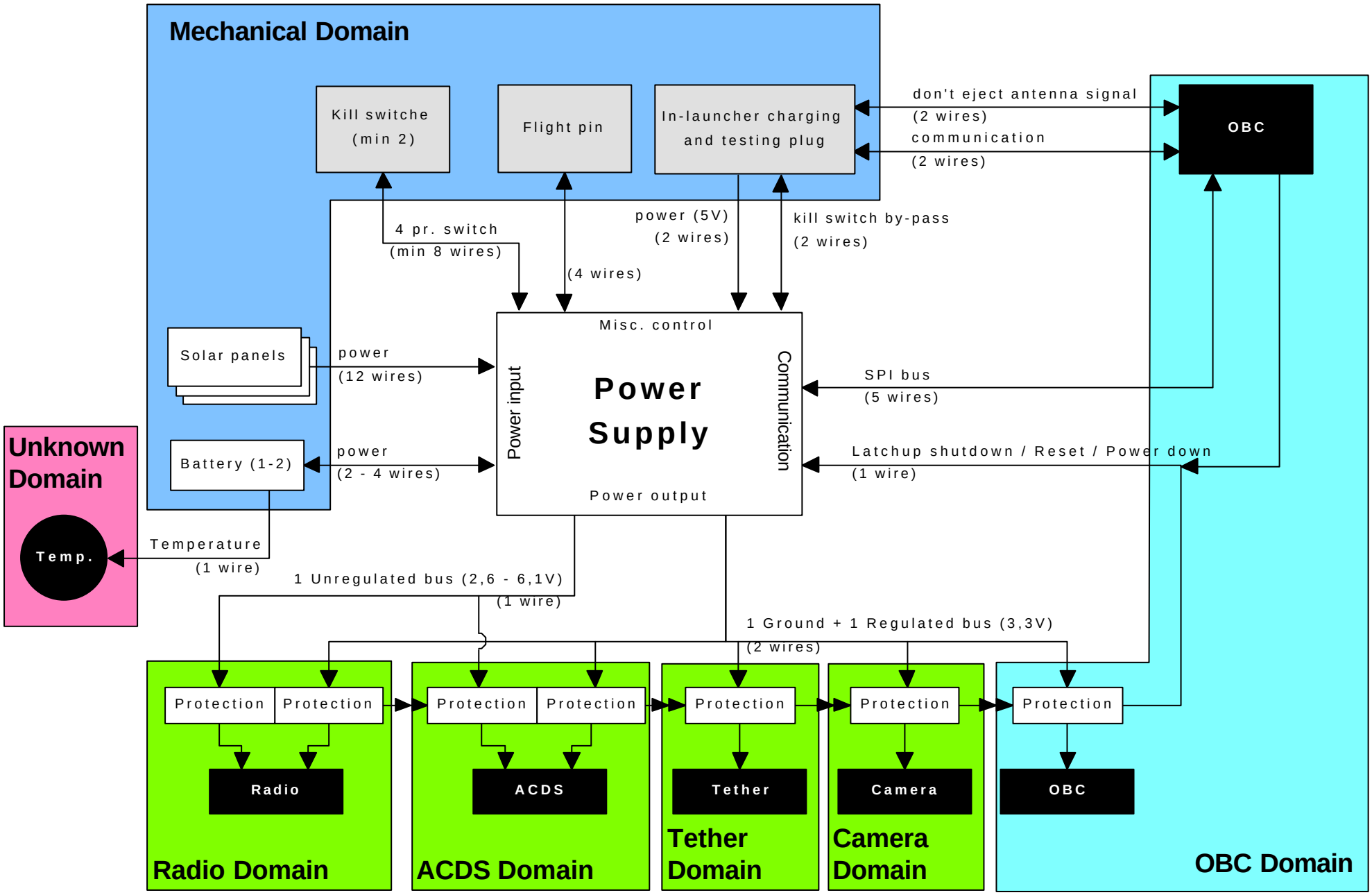

Satellite Panasonic 18650 1500mAh battery, in temperature test.
Capacity[mAh]
1600
1400
1200
1000
800
600
400
200
0
1513
0
308
1152
1421
1493
1511
1483
23
-40
-20
-10
10
35
55
23
°C
Discharge cap


CGR18650H temperature test, discharge
Voltage, V
4.500
4.000
3.500
3.000
2.500
2.000
1.500
1.000
500
0
Current, mA; Temparature, 1/10 °C
300
200
100
0
-100
-200
-300
-400
-500
0
0,5
1
1,5
2
2,5
3
3,5
4
4,5
5
Time, hours
Voltage
Current
Temperature

Appendix D - Electrical Interfaces

1 page

Power Subsystem Interfaces



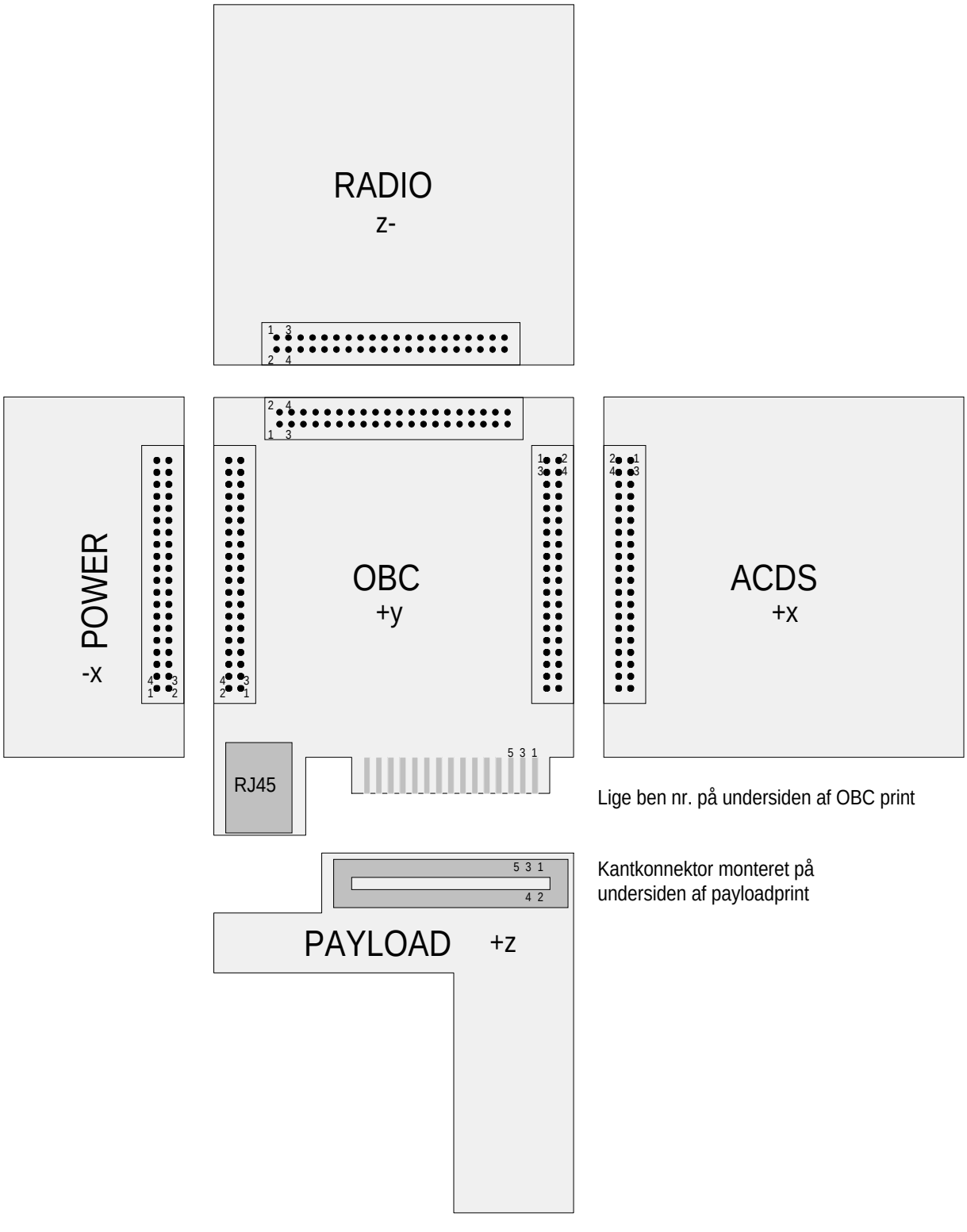
Appendix E - Pin 1 Locations

1 pages

DTUsat

Nedenstående figur viser hvorledes print er placeret i forhold til hinanden. Tegningen er set fra toppen af satelliten (+y), dvs. power-, radio-, acds og payload-printene skal foldes "nedad".

Tal ved stik angiver ben nr. Antal forbindelser i stikkene på tegningen passer ikke nødvendigvis med virkeligheden.



Lige ben nr. på undersiden af OBC print

Kantkonnektor monteret på undersiden af payloadprint

Appendix F - Sepic Spreatsheet

2 pages

Vin,min	2,6	V
Vin,typ	3,8	V
Vin,max	6	V
Vout	3,6	V
Iout	0,7	A
Freq:	100000	Hz
DeltaVOut	0,05	V
Rcp	0,05	ohm
Rl1	0,12	ohm
Rl2	0,12	ohm
Rsw	0,06	ohm
gamma	0,05	

Spolen:	uH	H	
Induktans:	100	0,0001	
uR	1490		
Al	36,6		
lj	28,6		
gab:	0,2	mm	
			actual:
antal vindinger, N:	36,69172		37
antal, begge spoler:	73,38345		74
wire dia:	0,3	mm	
h:	2,4	mm	
b:	6,3	mm	
antal vindinger pr. lag:	20		
antal lag:	8		
totalt antal vindinger:	160		

Calculations:

Period: 0,00001 s

eq 2: Ai = (Vout+Rsw*Iout)/Vin

	Aideal	Vin
Vin,min	1,400769	2,6
Vin,typ	0,958421	3,8
Vin,max	0,607	6

eq 3: Aa = (Vout + Rsw*Iout + Iout(Ai*Rcp+Rl2))/(Vin-Ai(RL1+Rsw)Iout-Rsw*Iout)
NB: RECURSIVE !!!

	Aactual	Aideal	Vin
Vin,min	1,605494	1,605	2,6
Vin,typ	1,037206	1,037	3,8
Vin,max	0,637724	0,6377	6

eq 4: a (dutycycle) = Ax/(1+Ax)

	a (dutycycl	Aactual
Vin,min	0,616196	1,605494
Vin,typ	0,509132	1,037206
Vin,max	0,389397	0,637724

eq 5: Iout = IL2

eq 6: IL1 = Aactual*Iout

	IL1	Aactual
Vin,min	1,123846	1,605494
Vin,typ	0,726044	1,037206
Vin,max	0,446407	0,637724

eq 7: Cp >= Iout*a(duty)min*T/(gamma*Vin,min)

Cp (min)	uF	gamma
3,32E-05	33,17977	0,05

eq 1:
Vcp(mean) = Vin

eq 8: Pcp=Aactual,min*Rcp*Iout^2

Pcp
0,039335

eq 9: Psw1=Aa,min*(1+Aa,min)*Rsw*Iout^2

Psw1
0,122983

eq 10: Prl1=Aa,min^2*Rl1*Iout^2

Prl1
0,151564

eq 11: Prl2=RL2*Iout^2

Prl2
0,0588

eq 12: Psw2=Rsw*Iout^2

Psw2
0,0294

eq 13: L1,min=2*T*(1-a(duty),max)*Vin,max/Iout

L1,min	uH
0,000105	104,6749

eq 14: IL1,sat>>Aa,min*Iout+0,5*T*a(duty),min*Vin,min/L1

IL1,sat	L1 chosen,	L1 chosen,H
1,203951	100	0,0001

eq extra: Id,max=IL1+Iout

ID1,max	
pulses	1,903951
mean	0,7

eq 15: L2,min=2*T*a(duty),max*Vin,max/Iout

L2,min	uH
6,68E-05	66,7537

eq 16: IL2,sat>>Iout+0,5*T*a(duty),max*Vin,max/L2

IL2,sat	L2 chosen,	L2 chosen,H
0,816819	100	0,0001

eq 17: Cout>=Aactual,min*Iout*a(duty),min*T/DVout

Cout,min	uF
0,000139	138,5018

eq 18: Cin=Cout/10

Cin	uF
1,39E-05	13,85018

eq 19: efficiency=Vout/Aactual*Vin

eff	Aa	Vin
Vin,min	0,862423	1,605494	2,6
Vin,typ	0,913385	1,037206	3,8
Vin,max	0,940846	0,637724	6

eq 20: VDS>1,15(Vout+Rsw*IOut+Vin)

VDS
11,0883

eq 21: VR > 1,15(Vout+Vin)

VR
11,04

Appendix G - Bill of Materials (BOM)

2 pages

Appendix G - Bill of Materials (BOM)

In order to be able to build the necessary test and flight models of the satellite it has been decided that we have to purchase 8 sets of components, namely for:

1 flight model
1 spare flight model
2 for radiation tests at Rigshospitalet
2 sets used for integration and mechanical/termical tests of the final setup
2 sets for repairs

For the final design the resistors, and most of the capacitors will be in a smaller package than 0805, but for now we're using these due to the easier assembly and handling.

Bill of Materials (prices are in dkr, EXCLUDING sales tax (25%)):

component	partno / value	reseller, order code	#pcs (1 set)	#pcs (8 sets)	price (dkr)	total (dkr)
Battery	CGR18650H	Sony / Merlin	1	8	260 @ 2	2080
Solar Cells		Emcore (?)			incl. tax:	6-70000
A/D converter	max1281BEUP	Maxim	2	16	42,0 @ 1k	*) 800,00
Bat. Charger	max1879EUA	Maxim	1	8	sample	*) 200,00
Current amp.	max4172EUA	Maxim	7	56	11,6 @ 1k	*) 675,00
Current amp.	max472ESA	Maxim	1	8	20,0 @ 1k	*) 160,00
dc/dc converter	Texas, TPS43000		1	8	sample	*) 400,00
uP opamp	Linear, LI1494IS8		1	8		
" replacement	ST, TS941ID	Farnell,out of stock	1	8	10,4 @ 5	*) 85,00
Switch	max890LESA	Maxim	1-2	8-16	10,0 @ 1k	*) 160,00
Temp.sensor		Maxim/Dallas	1-2	8-16		*) 200,00
Coil	Do-it-yourself		1	8	samples	
Connector	14 pin, doublerow	(28 pins total)	1	8	3,0 @ 1	24,00
P-FET	Vishay, Si9803		3	24	sample	*) 200,00
N-FET	Vishay, Si9804		1	8	sample	*) 100,00
Schottky	BAT54		1	8	sample	*) 100,00
	PRLL5817	Farnell 302-3280	6	48	3,38 @ 25	169,00
	ZHCS1000	Farnell 743-781	1	8	4,42 @ 5	44,20
Zener	LT1389		1	8	sample	*) 100,00
Capacitor 0805	220p	Farnell 755-590	1	8	1,000 @ 10	10,00
	1n	Farnell 753-580	1	8	0,572 @ 10	5,72
	4n7	Farnell 755-710	1	8	0,624 @ 10	6,24
	10n	Farnell 755-722	12	96	0,65 @ 25	65,00
	22n	Farnell 755-760	1	8	1,010 @ 10	10,10
	100n	Farnell 755-564	3	24	0,702 @ 25	17,55
	470n	Farnell 335-2043	3	24	1,040 @ 10	31,20
	2u2	Farnell 335-2092	1	8	1,130 @ 10	11,30
	4u7	Farnell 318-9053	2	16	5,20 @ 10	104,00
	10u		1	8		*) 150,00

continues

Bill of Materials, continued:

Component	Partno / value	Reseller, order code	#pcs (1 set)	#pcs (8 sets)	Price (dkr)	Total (dkr)
Capacitor 1210	40u, non polarized	Murata, GJ232NF 51A226ZD01L	1	8	n/a	
Capacitor, tantalium	100u, low ESR	Farnell 331-4066	1	8	14 @ 5	140,00
	200u, low ESR	Farnell 331-4078	1	8	25 @ 5	250,00
Resistor 1208	R051	Farnell 438-790	7	56	11,57 @ 5 8,32 @ 25	531,70
Resistor 0805, 0,1 %	3M57		1	8	n/a	*) 10,00
	3M		1	8	n/a	*) 10,00
	2M05		1	8	n/a	*) 10,00
	10M		1	8	n/a	*) 10,00
Resistor 0805	Assorted 1%		30	240	1 @ 10 *)	240,00
			Total, excluding solar cells:			7110,00
			Total, including solar cells:			77110,00

*) estimated price

sample = for now we're using free sample parts - and we don't now the pricing

Appendix H - PCB Layout Considerations

2 pages

Appendix H - PCB Layout Considerations

Some of the integrated circuits we're using are requiring special consideration when the PCB is routed. We've collected a list of these requirements in this section.

Max4172 (Current amplifier)

Rsense: Low inductance metal-film - prefered SMD.

Rout up to 200k results in minimal error. The input of an ADC must be much greater than Rout (100 x Rout) to avoid degrading measurement accuracy.

Single point star ground recommended for highest current measurement accuracy.

Optional decoupling:

1uF at Out to Gnd: Filters noise by current transients
Large C at RS (load side) to Gnd to decouple the load (reducing current transients)
1uF between RS+ and RS-: Can be filtered to average the sensed current

Max472 (Bi-directional current amplifier)

Rsense: Low inductance metal-film - prefered SMD.

Single point star ground recommended for highest current measurement accuracy.

Optional decoupling:

1uF at Out to Gnd: Filters noise by current transients
Large C at RS- (load side) to Gnd to decouple the load (reducing current transients)
1uF between RS+ and RS-: Can be filtered to average the sensed current

Max1879 (Battery charger)

Vin to Gnd: 100nF capacitor
VGS of PMOS < 2.5V
ADJ to Gnd: 1nF to 2 nF
BATT to Gnd: 1,5uF / amp of charge current) => 1uF is plenty for our 0,5 A

Max 1281 (A/D converter)

Don't run analog and digital signal lines parallel to one another
Don't run digital lines underneath the ADC package

Single point star ground recommended. Connect all analog grounds to the star ground at this point only. Connect the digital system ground to star ground at this point only

VDD1 to Gnd: 100nF AND 10uF capacitors (close to pin 20)
RefAdj to Gnd: 10nF
Ref to Gnd: 4,7 uF
VDD1 connected to VDD2 near the chip

Optional decoupling:

Channel decoupling, 10n

Max 890 (Current limited switch)

IN to Gnd: 1uF (ceramic) higher is ok
OUT to Gnd: 100 nF

Input and output capacitors as close as possible to the device (max 5 mm)

LT1494 (Op-amp)

100nF decoupling capacitor

TPS43000 (DC/DC controller)

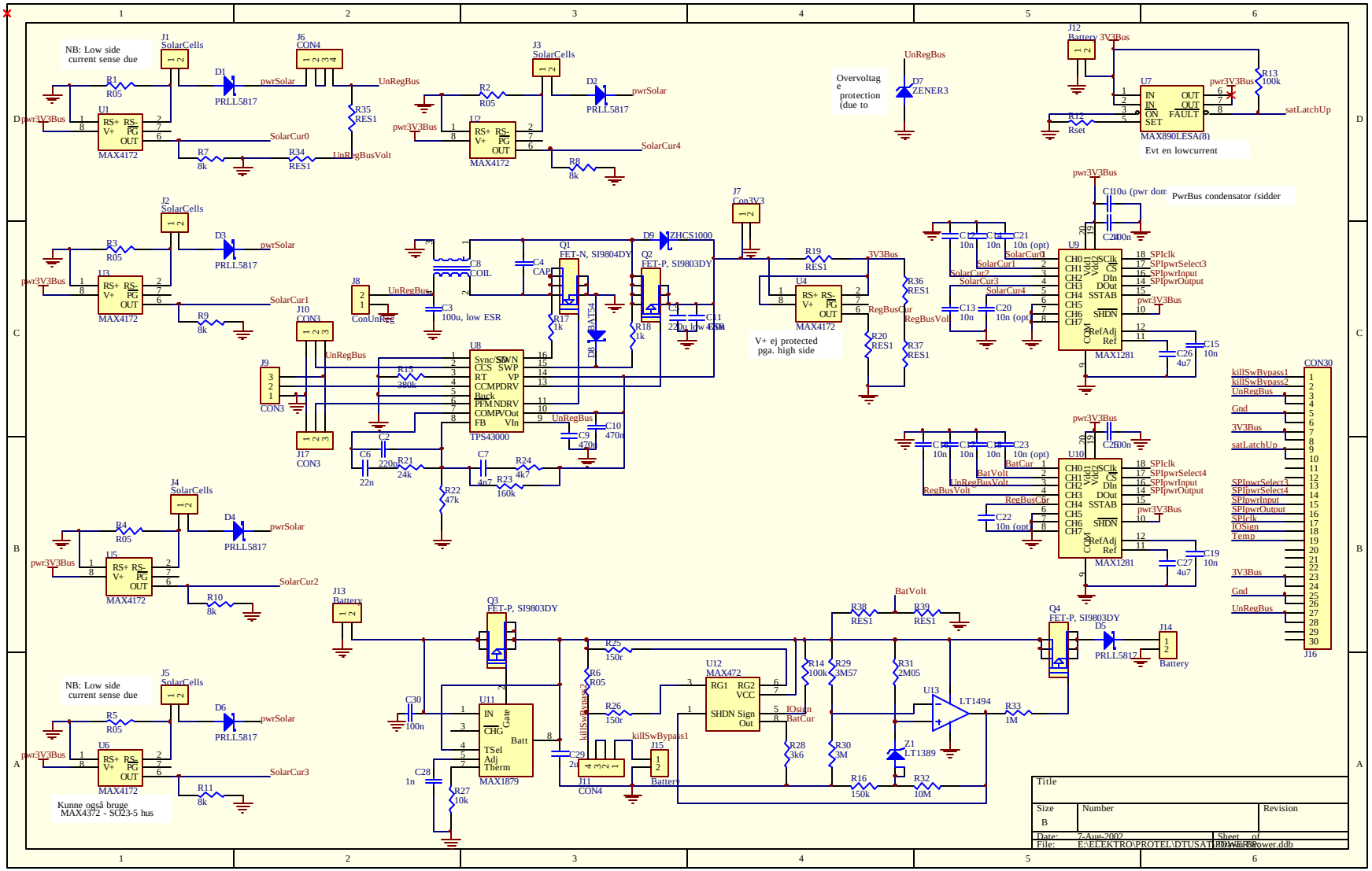
Feedback divider is especially susceptible to noise pickup
Layout should be as tight as possible
Feedback, compensation and timing components should be kept away from the power components (MOSFETs, inductor).
Keep all components as close to the device pins as possible.
Nodes that are especially noise sensitive are the FB, RT and COMP pins.
A ground plane is highly recommended.

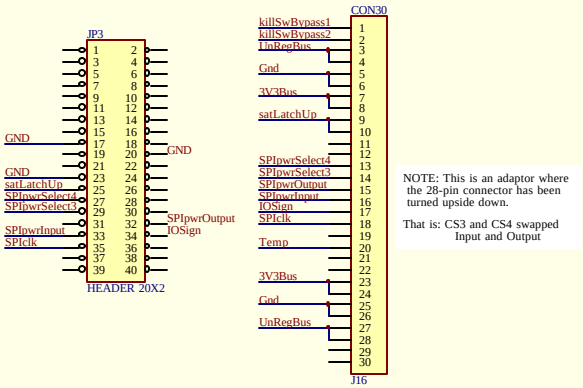
GND pin should be close to the source of the N-channel MOSFET, the input filter capacitor, and the output filter capacitor.
The grounded end of the RT resistor, the feedback divider resistor, and the SYNC/SD, CCS, CCM, \PFM\, and BUCK pins from the signal ground and should be connected to the quietest location of the ground plane (away from switching elements).

VIN to GND: 470nF (close to pin 9)
VOUT to GND: 470nF (close to pin 10)
VP to GND: 470nF (close to pin 12)

Appendix I - Schematics

2 pages


NB: Low side current sense due
J1 SolarCells
J6 CON4
D1 PRLL5817
pwrSolar
UnRegBus
R1 R05
U1 MAX4172
pwr3V3Bus
SolarCur0
R7 8k
R34 RES1
UnRegBusVolt
R35 RES1
J3 SolarCells
D2 PRLL5817
R2 R05
U2 MAX4172
SolarCur4
R8 8k
Overvoltage protection (due to
D7 ZENER3
J12 Battery 3V3Bus
U7 MAX890LESA(8)
R13 100k
R12 Rset
satLatchUp
Evt en lowcurrent
J2 SolarCells
D3 PRLL5817
R3 R05
U3 MAX4172
SolarCur1
R9 8k
J8 ConUnRegBus
C3 100u, low ESR
C8 COIL
C4 CAP
Q1 FET-N, SI9804DY
D8 BAT54
R17 1k
D9 MBRS1000
Q2 FET-P, SI9803DY
R18 1k
C11 220u low ESR
J7 Con3V3
R19 RES1
U4 MAX4172
3V3Bus
R36 RES1
R37 RES1
R20 RES1
RegBusCur
RegBusVolt
V+ ej protected pga. high side
C10u (pwr dom
PwrBus condensator /sidder
U9 MAX1281
SolarCur1
SolarCur2
SolarCur3
SolarCur4
SPIclk
SPIpwrSelect3
SPIpwrInput
SPIpwrOutput
C15 10n
C26 4u7
J9 CON3
J10 CON3
J17 CON3
U8 TPS43000
R15 380k
C2
C6 22n
220p
R21 24k
C7 4n7
R24 4k7
R23 160k
R22 47k
C10 470n
C9 470n
U10 MAX1281
BatCur
BatVolt
UnRegBusVolt
RegBusCur
SPIpwrSelect4
C19 10n
C27 4u7
CON30
killSwBypass1
killSwBypass2
UnRegBus
Gnd
3V3Bus
satLatchUp
SPIpwrSelect3
SPIpwrSelect4
SPIpwrInput
SPIpwrOutput
SPIclk
IOSign
Temp
J16
J4 SolarCells
D4 PRLL5817
R4 R05
U5 MAX4172
SolarCur2
R10 8k
J13 Battery
Q3 FET-P, SI9803DY
Q4 FET-P, SI9803DY
D5 PRLL5817
J14 Battery
R38 RES1
R39 RES1
BatVolt
R25 150r
R6 R05
killSwBypass2
R26 150r
U12 MAX472
R14 100k
R29 3M57
R31 2M05
U13 LT1494
R33 1M
IOSign
BatCur
R28 3k6
R30 3M
Z1 LT1389
R16 150k
R32 10M
J15
J11 CON4
killSwBypass1
Battery
C30 100n
C28 1n
R27 10k
U11 MAX1879
C29 2u
J5 SolarCells
D6 PRLL5817
R5 R05
U6 MAX4172
SolarCur3
R11 8k
Kunne også bruge MAX4372 - SO23-5 hus
Title
Size B
Number
Revision
Date: 7-Aug-2002
Sheet of
File: E:\ELEKTRO\PROTEL\DTUSAT\Boards\Power.ddb



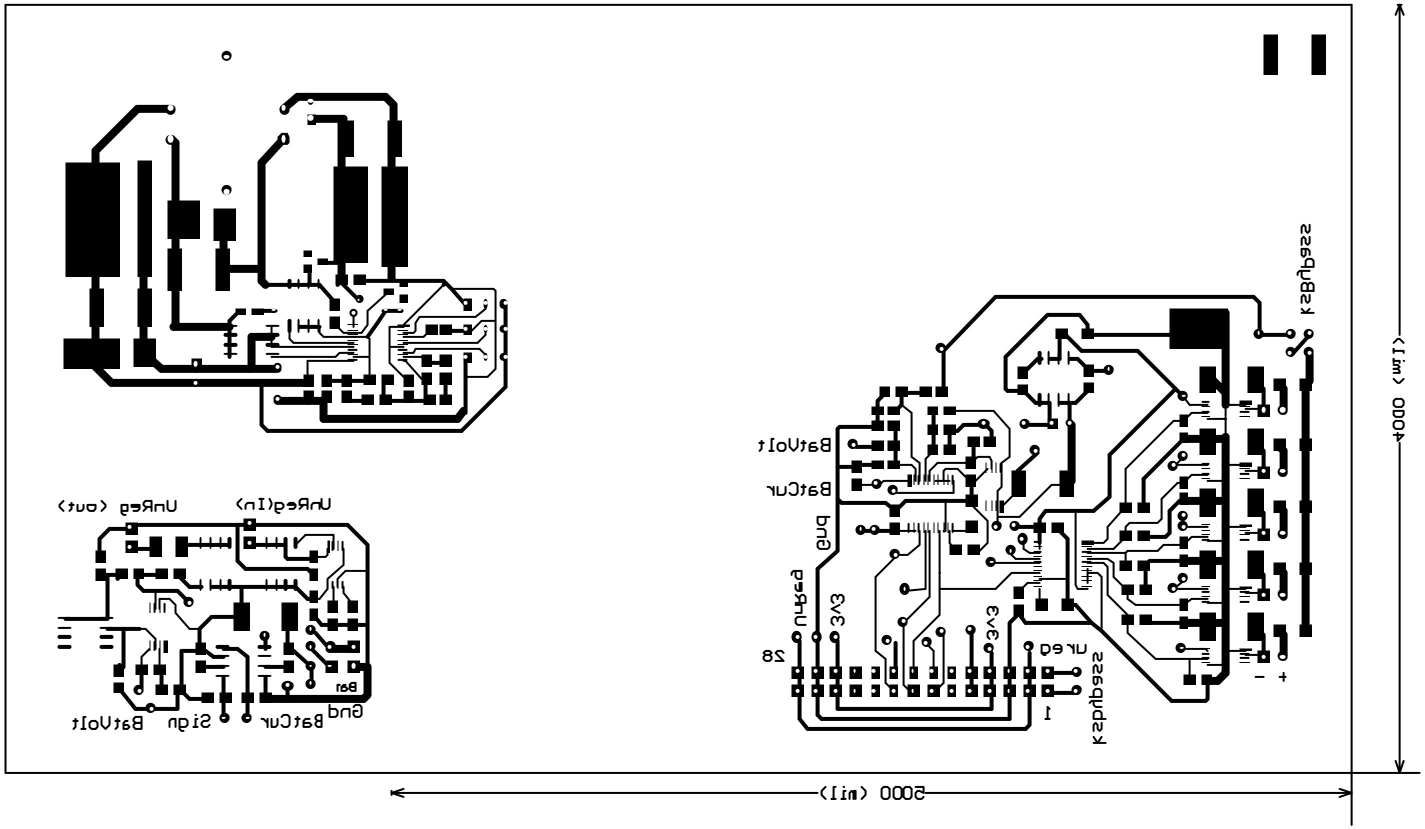
NOTE: This is an adaptor where the 28-pin connector has been turned upside down.

That is: CS3 and CS4 swapped Input and Output

Title		
Size B	Number	Revision
Date: 7-Aug-2002	Sheet of	
File: E:\ELEKTRO\PROTEL\DTUSAT\Power\Power.ddb		

Appendix J - PCB Layout

2 pages



DTUsat
Power
Group

TITLE: DTUsat Powersupply Prototype

ENGINEER: Michael
PHONE:

ENGINEER: Thomas
PHONE:

DATE: 7-Aug-2002

REV: 01

PART NO: 1

FILE NAME: 1Main.PCB

LAYER: Mechanical Layer 4

GERBER: .GTL

6.0
5.0
4.0
3.0
2.0
1.0
0
Y
X
0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
5000 (mil)
7000 (mil)
1
1
FILE NAME Connector.PCB
LAYER Mechanical Layer 4
GERBER .GBL
ENGINEER
PHONE
PART NO.
REV 01
DATE 7-Aug-2002
TITLE: Custom Made Board
ENGINEER
PHONE
PLACE
LOGO
HERE

Appendix K - Test software

3 pages

Appendix K - Test Software

```
program ISA4;

{ Program to test the max1281 adc }

uses
  Crt, Dos;

const
  base  = $340;

procedure Measure(Ch: byte; var Data: Word);
var
  A,b,i, ud : Byte;
  ind : word;
begin
{
  CS3:     341.2
  CS4:     341.1
  Din:     341.4 (in as seen from max1281)
  Clk:     341.5

  Sign:    341.4
  Dout:    341.3 (out as seen from max1281)
}
  Ud := ch shl 4;
  ud := Ud or $8F;

  a := $CD; { select adc }
  port[base+1] := a;
  for i := 1 to 8 do begin  { clock data into adc }
    b := a;
    if (ud and $80) <> 0 then
      b := b or $10;   { Din pin }
    port[base+1] := b; { set din }
    b := b or $20;     { clk pin }
    port[base+1] := b; { clk hi }
    b := b and not $20;{ clk pin }
    port[base+1] := b; { clk lo }
    ud := ud shl 1;
  end;
  ind := 0;
  for i := 1 to 16 do begin
    port[base+1] := $ED; { clk hi }
    port[base+1] := $CD; { clk lo }
    port[base+5] := 0;
    a := port[base+1];
    if (a and $8) <> 0 then
      ind := ind or 1;
    ind := ind shl 1;
  end;
  ind := ind shr 3; { skip tailing zero }
  Data := ind and $FFF;
  a := $FF; { select nothing }
  port[base+1] := a;
end;

procedure Measure2(Ch: byte; var Data: Word);
var
  A,b,i, ud : Byte;
  ind : word;
begin
{
  CS3:     341.2
```

```
  CS4:     341.1
Din:     341.4 (in as seen from max1281)
  Clk:     341.5

  Sign:    341.4
  Dout:    341.3 (out as seen from max1281)
}
  Ud := ch shl 4;
  ud := Ud or $8F;

  a := $CB; { select adc }
  port[base+1] := a;
  for i := 1 to 8 do begin  { clock data into adc }
    b := a;
    if (ud and $80) <> 0 then
      b := b or $10;   { Din pin }
    port[base+1] := b; { set din }
    b := b or $20;     { clk pin }
    port[base+1] := b; { clk hi }
    b := b and not $20;{ clk pin }
    port[base+1] := b; { clk lo }
    ud := ud shl 1;
  end;
  ind := 0;
  for i := 1 to 16 do begin
    port[base+1] := $EB; { clk hi }
    port[base+1] := $CB; { clk lo }
    port[base+5] := 0;
    a := port[base+1];
    if (a and $8) <> 0 then
      ind := ind or 1;
    ind := ind shl 1;
  end;
  ind := ind shr 3; { skip tailing zero }
  Data := ind and $FFF;
  a := $FF; { select nothing }
  port[base+1] := a;
end;

const
  Channel2Bin : array[0..7] of byte = (0,4,1,5,2,6,3,7);
  ss : string = '+-';
var
  A,X : Byte;
  data : word;
  sign : byte;
  s : longint;
begin
  clrscr;
  a := 1;
  repeat
    port[base+5] := 0;
    sign := (port[base+1] and $10) shr 4;
    if sign = 1 then s := -1 else s := 1;
    gotoxy(1,1);
    if sign = 1 then
      write('Bat Sign:      ',sign,' = discharging')
    else
      write('Bat Sign:      ',sign,' = charging');
    clreol; writeln;

    Measure(Channel2Bin[0],data);
    write('Bat Cur:       Ch ',0,' = ',data,'   ');
    gotoxy(30,wherey); write(' = ',2.5/4095*data:2:3,' V');
    gotoxy(45,wherey); write(' Adjusted = ',s*2.5/4095*data/1.462*1000:5:0,' mA');
    clreol; writeln;
```

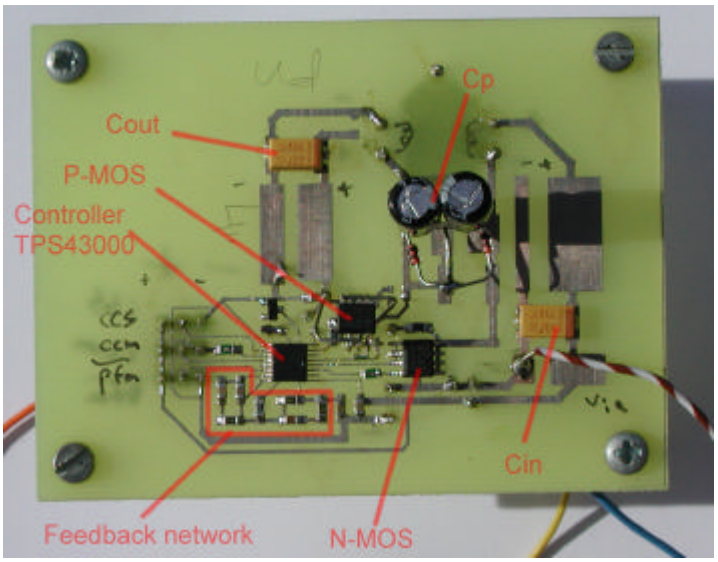
```
    Measure(Channel2Bin[1],data);
    write('Bat Volt:      Ch ',1,' = ',data,'   ');
    gotoxy(30,wherey); write(' = ',2.5/4095*data:2:3,' V');
    gotoxy(45,wherey); write(' Adjusted = ',2.5/4095*data*2.00:2:3,' V');
    clreol; writeln;

    Measure(Channel2Bin[2],data);
    write('UnRegBus Volt: Ch ',2,' = ',data,'   ');
    gotoxy(30,wherey); write(' = ',2.5/4095*data:2:3,' V');
    gotoxy(45,wherey); write(' Adjusted = ',2.5/4095*data/0.344:2:3,' V');
    clreol; writeln;

    Measure(Channel2Bin[3],data);
    write('RegBus Volt:   Ch ',3,' = ',data,'    ');
    gotoxy(30,wherey); write(' = ',2.5/4095*data:2:3,' V');
    gotoxy(45,wherey); write(' Adjusted = ',2.5/4095*data*2.00:2:3,' V');
    clreol; writeln;

    Measure(Channel2Bin[4],data);
    write('RegBus Cur:    Ch ',4,' = ',data,'   ');
    gotoxy(30,wherey); write(' = ',2.5/4095*data:2:3,' V');
    gotoxy(45,wherey); write(' Adjusted = ',2.5/4095*data/2.856*1000:5:0,' mA');
    clreol; writeln;

    for a := 5 to 7 do begin
      Measure(Channel2Bin[a],data);
      writeln('Unused:        Ch ',a,' = ',data,'             ');
    end;

    gotoxy(1,15);
    for a := 0 to 4 do begin
      Measure2(Channel2Bin[a],data);
      write('Cell ',a,':        Ch ',a,' = ',data,'   ');
      gotoxy(30,wherey); write(' = ',2.5/4095*data:2:3,' V');
      gotoxy(45,wherey); write(' Adjusted = ',2.5/4095*data/3.468*1000:5:0,' mA');
      clreol; writeln;
    end;

    for a := 5 to 7 do begin
      Measure2(Channel2Bin[a],data);
      writeln('Unused:        Ch ',a,' = ',data,'             ');
    end;

  until keypressed;
  a := $FF; { select nothing }
  port[base+1] := a;
end.
```

Appendix L - Pictures of the Prototype

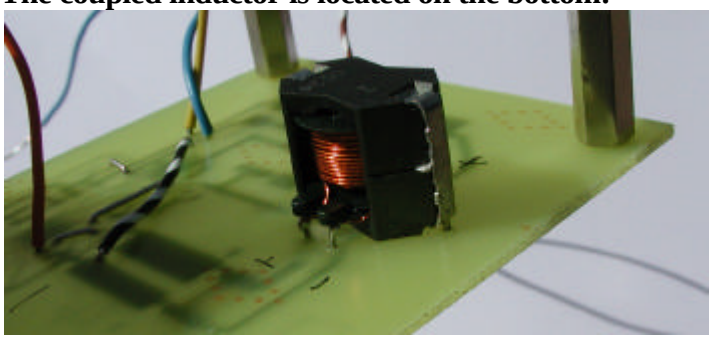
2 pages

Appendix L - Pictures of the Prototype

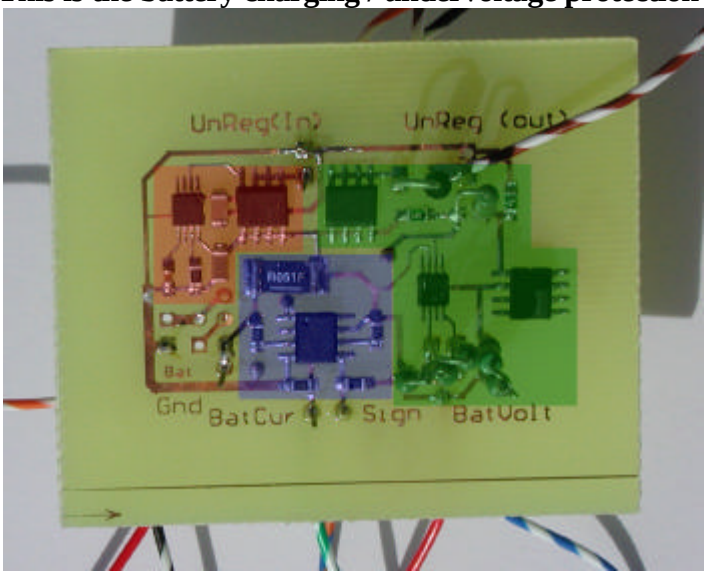
This is the DC/DC converter:



The coupled inductor is located on the bottom:



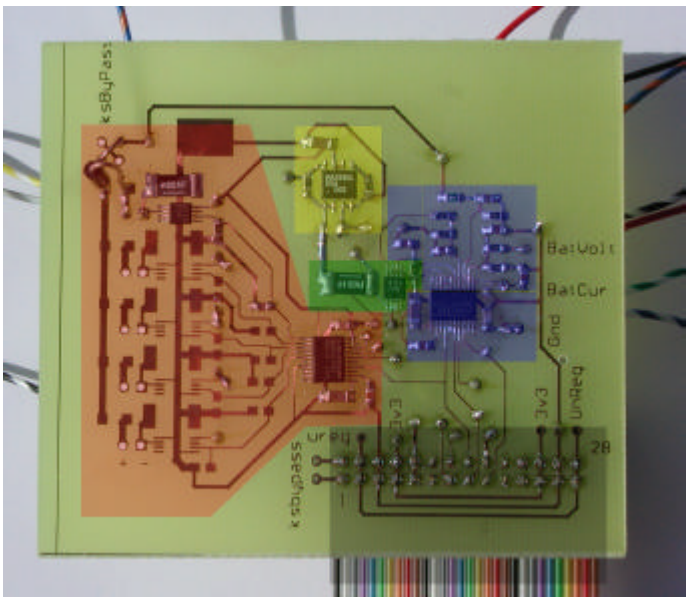
This is the battery charging / undervoltage protection circuit:



Legend

Red - MAX1879 Battery charger
Blue - Current measurement
Green - Undervoltage protection

This board includes current measurements of the regulated bus, and of the input current from the solar cells. Also voltage dividers are located on this board:



Legend

Red - Current measurement for solar input power
Yellow - Local latchup protection
Green - Current measurement of regulated bus
Blue - Voltage measurements, incl. ADC
Black - Interface