The Design of an Efficient, Elegant, and Cubic Pico-Satellite Electronics System

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In Partial Fulfillment
of the Requirements for
Master of Science in
Electrical Engineering

By
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ABSTRACT

The Design and Testing of an Efficient, Elegant, and Cubic Pico-Satellite Electronics System

By Christopher Alan Day

1kg satellites, called CubeSats, are small and cheap enough that most universities are able to design and build them as fully functional satellites. Designing satellite systems in this new, small, and light-weight design presents a new challenge to satellite developers. This thesis describes the design of a flexible electronic power system (EPS) and Command and Data Handling (C&DH) system capable of interfacing to many different payloads.

The power system is designed to be robust with a fault tolerant architecture. The solar panels are individually peak power tracked for optimal performance and are each fused for short circuit protection. Redundant batteries are used with individual safety circuits so that if either battery has an internal short or open, that battery can be disconnected from the power bus and the other battery can continue to operate normally. The electrical loads are isolated from each other through the use of multiple DC-DC converters and "smart fuses."

The C&DH system is designed with a two wire serial bus that transports critical data between more than 20 devices on the spacecraft. The C&DH processor controls data flow on the bus and is able to isolate bus branches in case a failure prevents bus

operation. Nine data acquisition circuits throughout the satellite monitor over 70 different sensors giving satellite health and status.

By designing circuits that mirror the operation and capability of larger and more complex satellite systems, CubeSats such as this are able to distribute power, communicate with ground stations, and perform scientific missions in much the same way as their larger brethren.

The power system and C&DH system described in this thesis has been built into the CubeSat CP2. CP2 has been built and is currently under final testing at Cal Poly. The design modifications listed in chapter 4 of this thesis represent most of the important design modifications on CP2's electronics at the time this thesis is written.

ACKNOWLEDGMENTS

I would like to thank all of the teachers and professors who have instilled in me analytical and creative knowledge.

I would like to thank my parents and extended family for raising me into the individual that I am today.

Most importantly, I would like to thank the Creator of the electron who has made this work possible and whose name I praise.

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1 Introduction

1.1 What are CubeSats?

A joint project between Cal Poly and Stanford created a satellite design standard that is feasible for most universities to build to. This satellite standard, called a CubeSat, is a cube 100mm on each side and has a mass of 1000g or less.

By making a very small and lightweight satellite to this specification, universities receive several advantages. The university can join a CubeSat development community where information on CubeSat design and construction can be shared. Mutual assistance enables universities that have no previous satellite building experience to create a CubeSat. Universities do not need to design or build a satellite deployment mechanism because that work has been completed by Cal Poly to facilitate CubeSat launches. Furthermore, the cost of the satellite launch is reasonable, at about $40,000.

The operation of CubeSats vary greatly. The specification is flexible enough that almost any payload that can fit in the satellite can be flown. Payload possibilities include radiation sensors, pulse-power devices, sun position sensors, and earthquake research sensors. Flying a payload is usually not the objective of building a CubeSat. The objective of most CubeSat development is to expose students to the full life-cycle development process of a satellite.

1.2 Changes from Traditional Satellite Designs

The design of a CubeSat satellite is very different from the design of a much larger satellite. Most satellites have a mass of hundreds of kilograms or more. These satellites are built with many complex redundant systems in order to increase the probability of mission success. Instead of having one C&DH processor, for example, they may have eight of them and a system of computer voting is implemented such that a majority of computer votes determines the next action. With such mass available to traditional spacecraft, the electronic systems they use are extremely complex and do not shrink well into Nano or Pico-satellite systems.

When designing Pico-satellites such as CubeSats, most of the electronic designs are not miniature versions of the complex electronics in larger satellite brethren. The designs are reinvented instead. If there isn't room for multiple C&DH processors in the CubeSat, the satellite could be designed with one processor and the ability to operate with limited functionality in case that processor fails. Redundant battery charging circuits may be used on larger satellites in order to increase the probability of a successful power system. On a CubeSat, a simple battery charging mechanism could be designed which is small enough that it fits into each solar panel. With this new system, if any of the solar panel battery chargers fail, the power from that solar panel will be lost but the power from the other solar panels would still work.

When CubeSats are designed, the design must be a simpler one than that used in a larger satellite. This simpler design will have more single point failures and a larger probability of mission failure than larger satellites but the higher probability of failure is known and accepted by the CubeSat community. With a smaller total mass, short development time, small workforce, and a cost budget several orders of magnitude lower than a traditional satellite, CubeSats require a non-traditional approach to satellite design.

1.3 Advances from CP1 to CP2

CP1 was the first CubeSat satellite designed at Cal Poly. The design objective of CP1's electronics was to build basic power distribution, data collection, data processing, and radio functions into a satellite. CP2 builds on the knowledge learned from CP1 to provide greater capability in its subsystems and to work with a range of payloads.

The electronic power system (EPS) on CP1 was simple, but functional. The solar panels were electrically brought together with isolation diodes and were then connected to the main power bus. CP2's design incorporates individual peak power tracking on every solar panel. This design allows each solar panel voltage to reach its optimal value, rather than track the battery voltage.

CP1 used two sets of batteries, one lithium primary battery to provide several days worth of energy in the event of a complete solar power failure, and a set of three Li-ion secondary batteries for ample solar energy storage. This design allows functionality with simplicity. CP2's design entails two Li-ion secondary batteries, almost identical to those used on CP2, each connected in parallel with the main power bus and each with individual battery protection circuits. This design provides a lower battery mass than CP1 but at the expense of lower total energy storage. With a lower battery mass, more of the total satellite mass can be attributed to the payload.

The load power conditioning on CP1 included individual DC-DC converters for the processor and each of the two transceivers. Having individual converters for the transceivers provided a level of redundancy so that one converter or one transceiver can fail as an open circuit, but the satellite can still communicate with a ground station. CP2 is designed with the same kind of redundancy but on a larger scale. There are three DC-DC converters, one for the C&DH system and one for each of the communication systems, much like CP1. The outputs of the DC-DC converters are sent through one or more smart fuses that will disconnect the power to a load momentarily if the load exceeds a programmed current threshold. By using multiple smart fuses, load branches that consume excessive current due to radiation damage do not affect other load branches, thus minimizing the effects of radiation.

The Command and Data Handling (C&DH) system and the Data Acquisition system used on CP1 is designed specifically to acquire data from its sun position sensor payload and to determine its own health status. This required a multiplexing Data Acquisition system to acquire 32 different analog voltages and encode that information for data transmission to earth. The design for CP2 is more generic. CP2 will acquire its own health status and work with a variety of payloads by providing a serial bus for flexible acquisition of data. When a payload for CP2 has been determined, a simple interface circuit will be built into the payload interface board that will acquire payload data in the format required for the particular payload and transmit that data on the serial bus.

The design of CP1 was extremely useful in determining the design requirements for CP2. By building CP1, the needs for CP2 where uncovered and addressed.

2 Electronic Power System (EPS)

2.1 Design of the Power System

CP2's power system must supply power, properly conditioned, to all electrical systems, as they need it. This means that the varying voltage from the solar panels, the varying voltage of the battery, and the precise voltage required by the processors and other loads must all be reconciled. Loads require proper voltage regulation and must be provided with fuses or similar circuits to protect the power supply.

The main objectives of the power system for CP2 are:

1- Maximize the power available to the payload
2- Maximize resilience to SELs (Single Event Latchups)
3- Isolate failures from causing other systems to fail
4- Operate with a high energy and space efficiency

In order to meet these goals, designs tailored for pico-satellites will utilize the latest in highly integrated and energy efficient technology. Circuit board space is limited inside a small satellite. The CP2 design uses circuit boards as the sides of our satellite, thereby providing much more circuit real estate than if the sides had been part of the aluminum structure. It uses a battery protection circuit that not only disconnects the batteries to prevent damage, it also detects battery voltage, current, accumulated current, and

temperature with just 2 ICs and a few passive components. For voltage conversion, the circuit uses highly efficient DC-DC converters designed for low power embedded applications. Figure 1 is a block diagram of the power system.

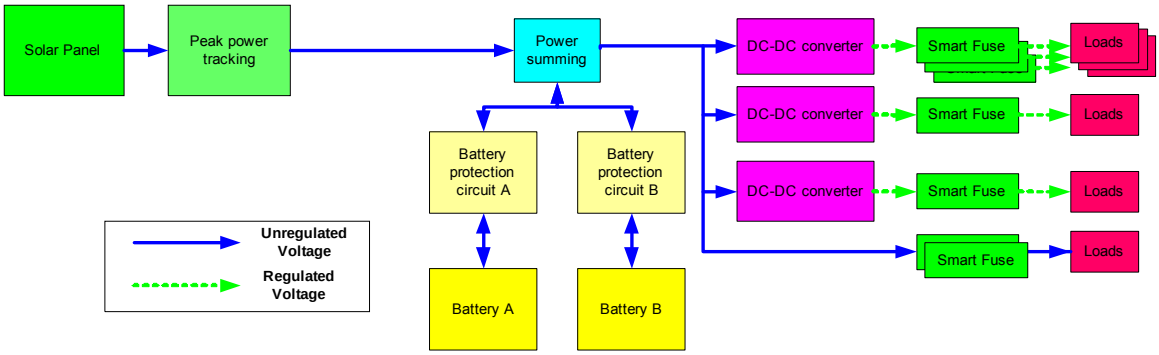

Figure 1. Energy flow diagram from the solar panels to the energy storage circuit, then to the DC-DC converters, smart fuses, and loads.

The final power system design is implemented on an 82 x 82 mm circuit board. The primary side is shown in Figure 2 and contains the DC-DC converters, smart fuses, and Remove Before Flight switch. The secondary side is shown in Figure 3 and contains the batteries. These images are of test boards and are not shown in flight configuration.

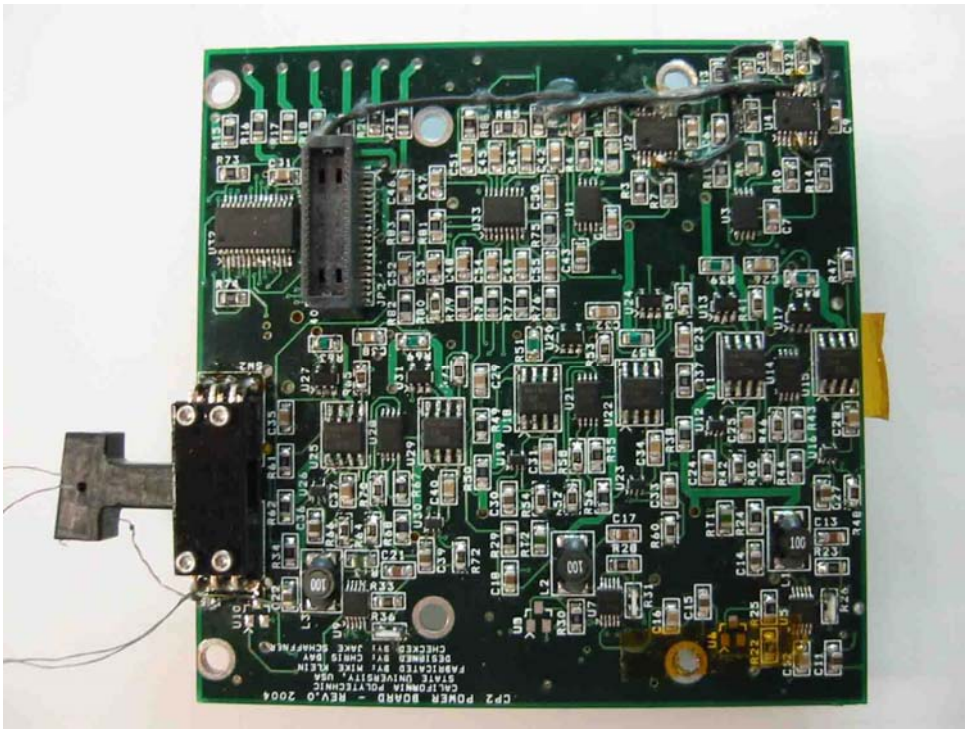

Figure 2. Power Board Primary Side.

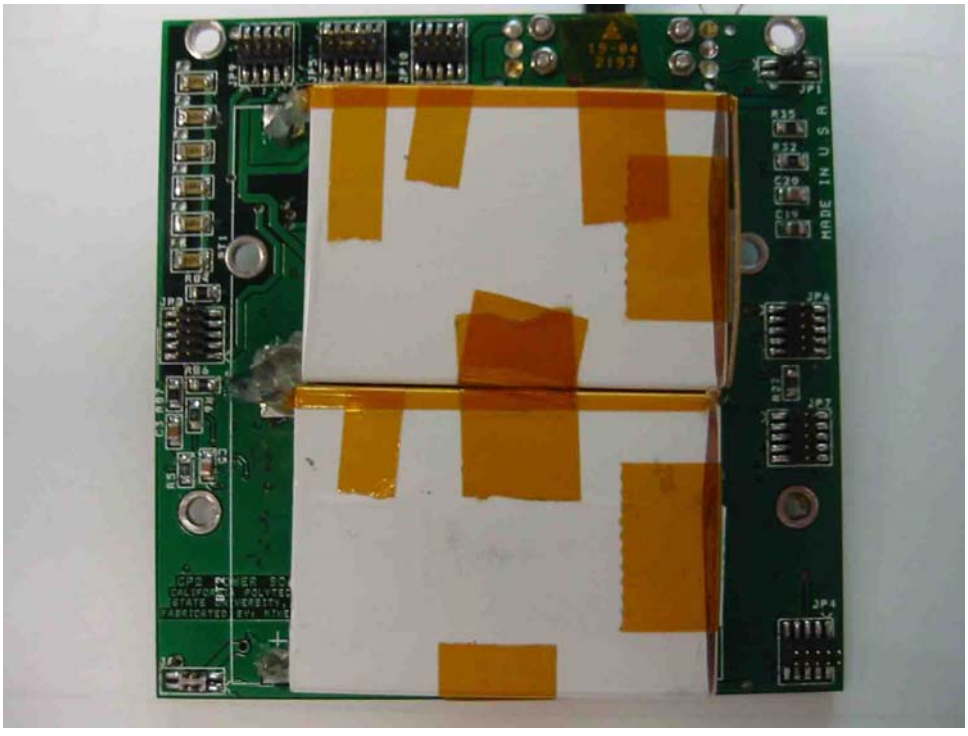

Figure 3. Power Board Secondary Side.

The side panels are implemented on a 100 x 82 mm circuit board. The primary side of the side panel contains two solar cells and one thermistor. The primary side of the side panel is shown in Figure 4. The secondary side of the side panel contains the MPPT system, Attitude control, and side panel data acquisition. The secondary side is shown in Figure 5. These test boards are shown with conformal coating but are not in flight configuration.

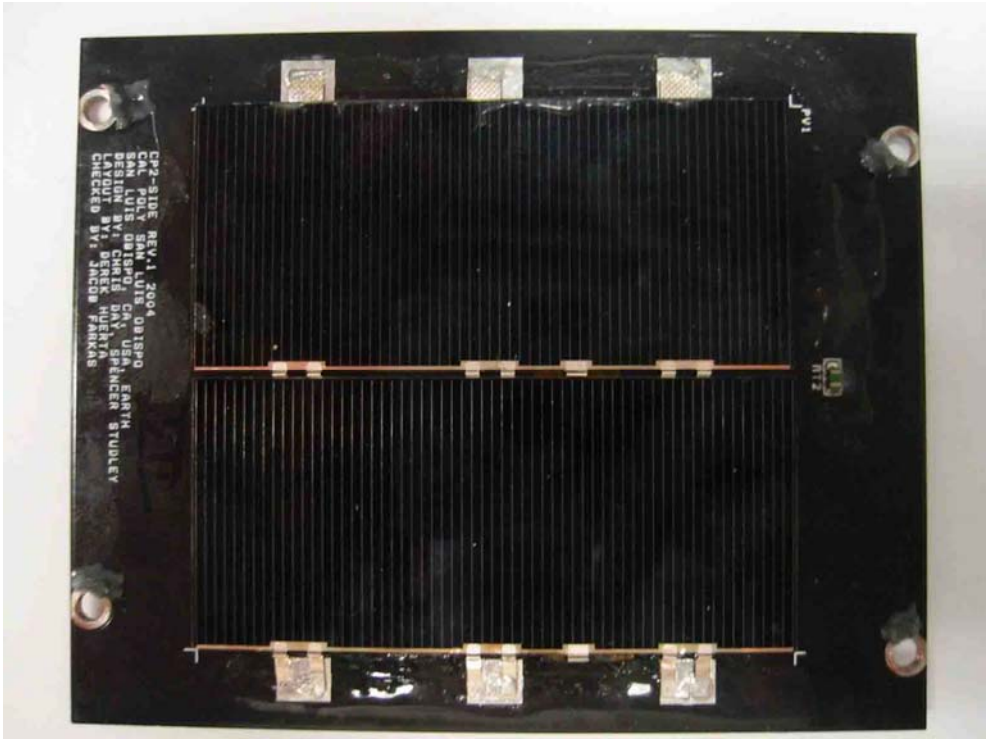

Figure 4. Primary Side of Side Panel.

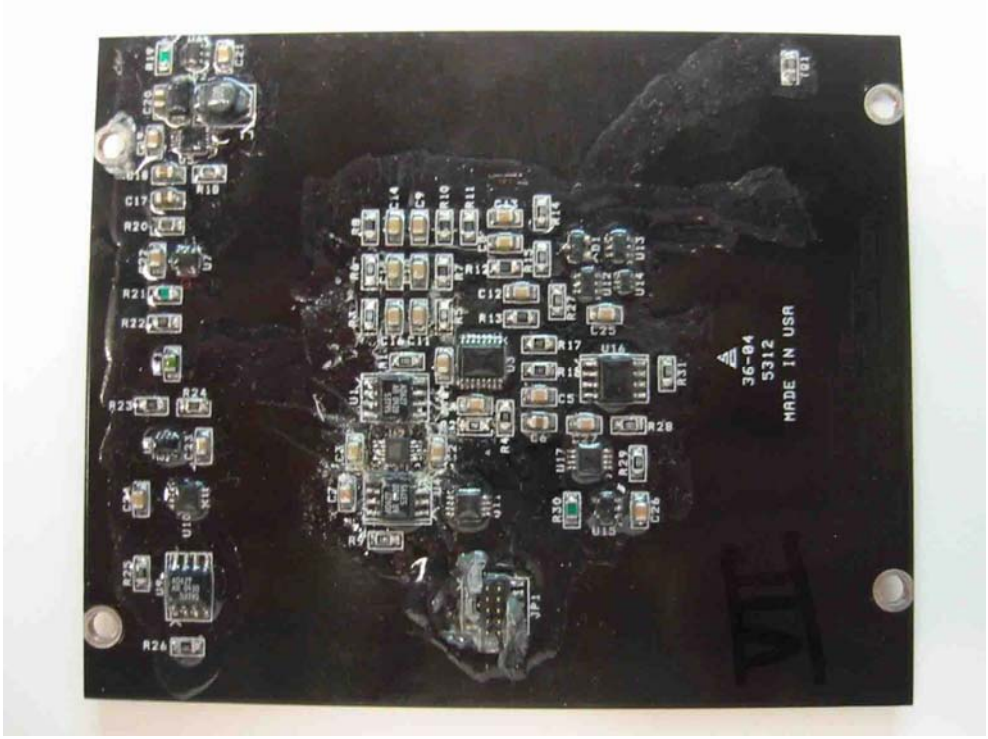

Figure 5. Secondary Side of Side Panel.

2.2 Solar Panel Power and MPPT

The solar panels on CP2 are the only method of receiving power for charging the batteries and powering the loads. Receiving power from the solar panels is therefore one of the critical points, and a single point of failure, of the satellite's operation. The design of CP2 should have power production from each solar panel as isolated from the other panels as possible to decrease the number of single points of failure.

The solar panels are the same model as used on CP1. They are the 505030 dual junction GaAs cells from Spectrolab. This model provides around 21.5% efficiency, a 2.09V per

cell voltage, and around 275mA of current output. With two cells in series, a power output of just over 1W is attained. Because the cells performed adequately for CP1 and we have a design heritage with using these cells, we decided to use them on CP2 as well.

2.3 Maximum Power Point Tracking (MPPT)

Solar panels love operating at cold temperatures. At cold temperatures, a solar panel can operate at higher voltages and produce more power. As a solar panel gets hot, it can only operate at lower voltages. Thus, maximum operating voltage and power are achieved with a cool solar panel. Figure 6 shows the effects of temperature on the current-voltage curve of a solar cell. As the temperature decreases, the cell's open circuit voltage increases. More importantly, the peak power point voltage of the solar panel will increase. The peak power point is the operating point of a solar panel that produces the maximum power output. It is also a very dynamic point that changes with the temperature, luminescence level, age, and radiation absorption of a solar cell.

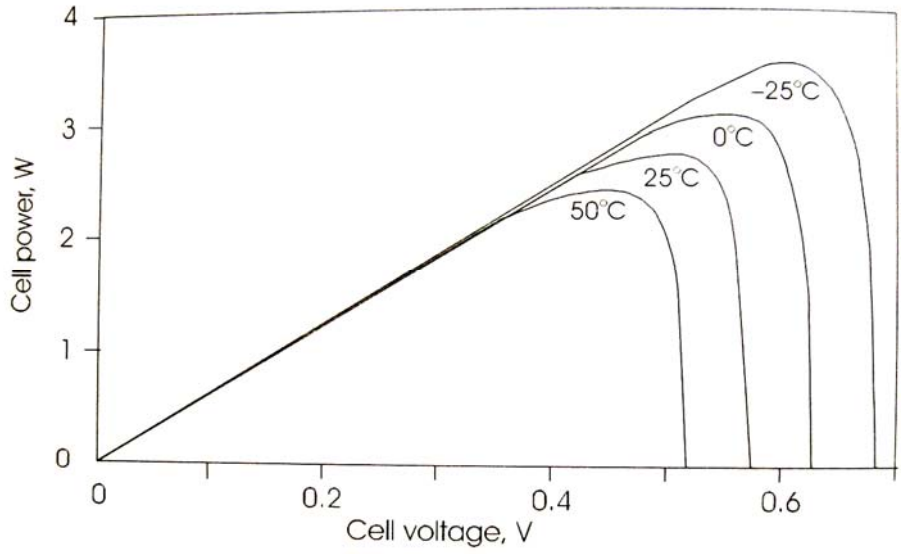

Figure 6. The P-V curves measured at different temperatures demonstrates the significant change in the voltage set point giving maximum power.[1]

The most common terrestrial method to operate a solar panel is with the solar panel operating voltage significantly below the peak power point voltage. Operating at this point allows the solar panel to produce a nearly constant and reliable output power regardless of cell temperature. This simple method of solar panel voltage regulation is usually accomplished by attaching the solar panel to a battery through a charge controller. With this method, the solar panel voltage also varies with the battery voltage.

Applying this method of solar panel operation, the solar panel is set to a sub-optimal voltage that varies as a direct result of battery voltage variation. A higher solar panel power occurs when the battery is fully charged and creates a high solar panel voltage.

This is contrary to requirements, since high solar panel power is most needed when the battery is discharged, not when it is charged.

Although this method of operating a solar panel is not optimal, it was the method employed on CP1 and achieved energy efficiency up to 90% of that achieved at the maximum power point.

To maximize the energy from a solar panel, it can be operated at its peak power point continuously, using a Power Point Tracker (PPT). This requires a system that determines the peak power point and constantly keeps the solar panel operating there. To accomplish this, a circuit is required to determine the power coming out of the solar panel. Another circuit is required to hold the solar panel at a constant voltage or current set point. Then, a processor or complex analog circuit is needed to modify the set point in order to find the highest power.

A preferred design for a CubeSat would use devices that the satellite will already need for other tasks. For example, current and voltage sensors will already be needed by the C&DH system to log solar panel performance. These same sensors can also be used to determine the solar panel power output for the PPT. The C&DH processor that collects the solar panel current and voltage data can also determine the solar panel power level and could change the solar panel's voltage set point. The only additional parts required are a circuit that holds the solar panel at a steady voltage and a DC-DC converter that converts power from the solar panel voltage to the CP2 main power bus voltage.

2.4 The Peak Power Tracking (PPT) System Used

A block diagram of the PPT system is displayed in Figure 7. The solar panel power is given to a TI TPS62000 DC-DC converter that converts the solar panel voltage to the battery voltage. The DC-DC converter output voltage and current are then sensed and read by the main processor. The main processor calculates the VI product using an algorithm to adjust the voltage set point so as to maximize this product. The voltage set point keeps the DC-DC converter's input voltage at a constant voltage. A design using these components is very space efficient because each of these blocks is already required for a different function, except for the voltage set point block.

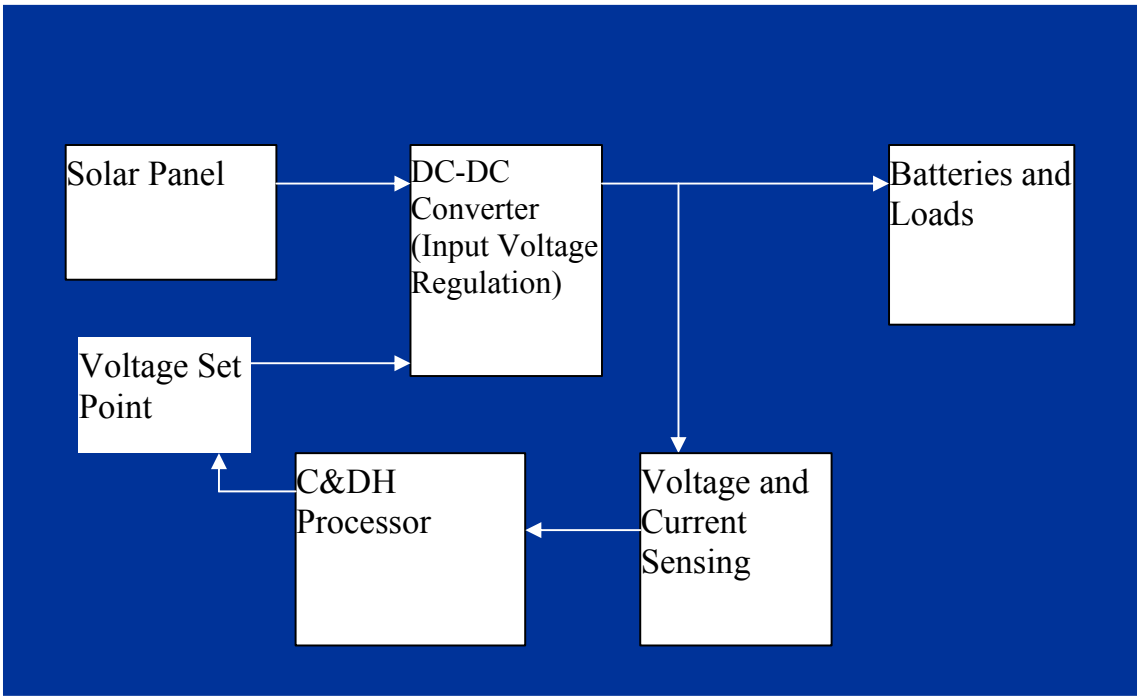

Figure 7. Block diagram of Maximum Power Point Tracking (MPPT) system.

2.4.1 DC-DC Conversion

The DC-DC converter is placed in between the solar panel and the CP2 bus to allow the battery voltage on the bus to be independent of the solar panel voltage. A simplified schematic for the modified DC-DC converter and voltage set point circuit is in Figure 8. The C&DH processor sets the solar panel set point voltage by changing the potentiometer value. The potentiometer, R37, and the fixed resistors R33 and R34, create a voltage divider that determines what solar panel voltage is required to turn on the MOSFET, Q1. The Digipot is an AD5245 from Analog Devices and can switch between 256 potentiometer values based on I^2C commands and employs solid-state technology. MOSFET Q1 and the resistor, R35, create a simple N-MOS inverter with a resistive load. The output of this inverter is fed to the feed back input of the DC-DC converter, U22. The inductor, L3 completes the DC-DC converter circuit with the switching performed internal to the TPS62000.

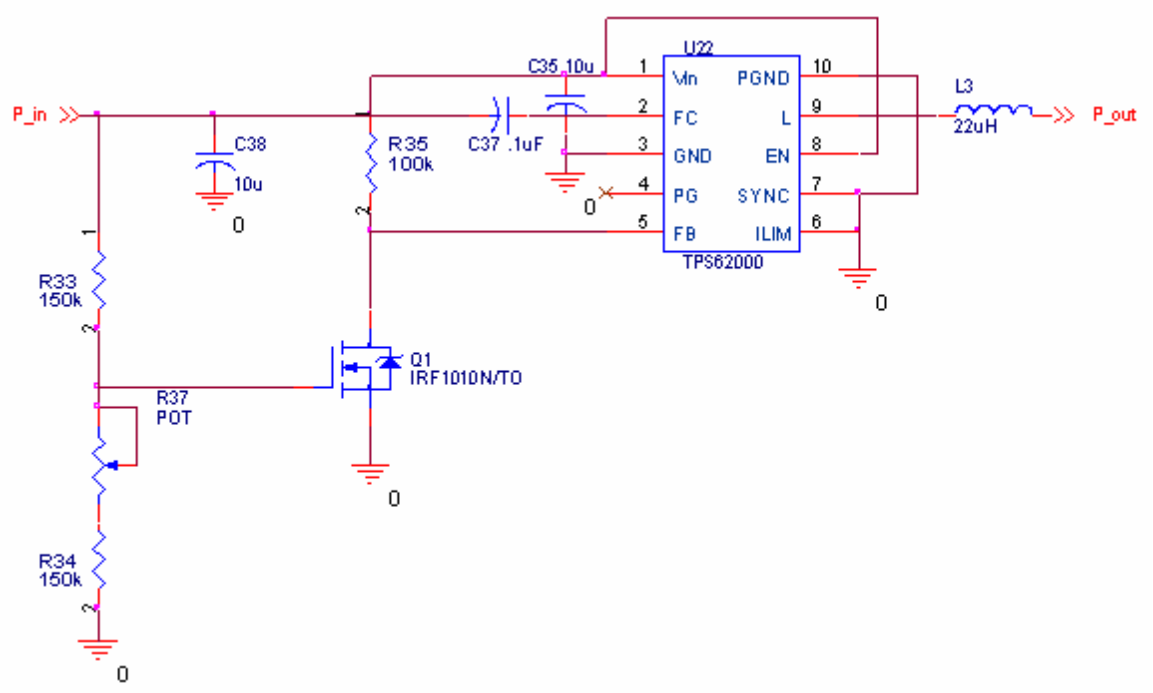

Figure 8. DC-DC converter and voltage set point schematic. (Simplified)

The operation of this circuit can best be explained from the end to the beginning. The DC-DC converter IC, U22, tries to move energy from its input to the output (the right side) of L3 whenever the feedback line, FB, is below about 0.45V. Whenever the feedback line is above 0.45V, it turns off. This means that if we want to regulate the output voltage to a set point we need only use a resistor divider to divide the desired output voltage down to 0.45V and feed the divided voltage into the feedback line. Then the DC-DC converter will turn on whenever the output is below the set point. For our design, we need to regulate the input voltage but using a simple voltage divider on the input and sending the divided voltage to the feedback line will not work.

We want the DC-DC converter to turn on and move energy away from the solar panel whenever the solar panel voltage increases above the set point. If we use a voltage divider on the input and send the divided voltage to the feedback line, the DC-DC converter will turn on whenever the solar panel voltage is below the set point. This is the opposite response that we need! The solution is, in essence, to invert the signal. A simple NMOS inverter with a resistor pull-up is used to invert the signal from the voltage divider. With this inverter in place, the system works properly. When the solar panel voltage is above the set point the MOSFET turns on, the voltage at the drain of the MOSFET drops, the feedback voltage goes low, and the DC-DC converter turns on.

2.4.2 Voltage and Current Sensing

The data acquisition circuit must be designed for the maximum measured current. The maximum current output can be found using the maximum power of the solar panel and dividing by the lowest battery voltage that the PPT system will operate with. The result is the maximum current given by the PPT output. The maximum solar panel output power is 1.13W and the minimum battery voltage for the satellite to operate is approximately 3.4V. This gives a maximum calculated current of 332mA. 350mA will be used as the maximum current to be measured as it allows a safety margin in case the solar panel performs better than expected or a lower battery voltage than the minimum occurs during data acquisition.

Maximum MPPT output current = (Solar panel power)/(min battery voltage) (equ. 1)

A simplified diagram of the general voltage and current sensing circuit is shown in Figure 9. The output current is measured using a 0.05 Ω resistor, R62. The resistor causes a voltage drop equal to 50mV per amp of current. The voltage is then amplified using the MAX4372H IC from Maxim. The MAX4372H acts as a special instrumentation amplifier and produces an output voltage proportional to the differential input voltage multiplied by a fixed gain. The Maxim IC amplifies the voltage by 100V/V. This means that the voltage measured at R3 and the voltage going into pin 8 of the MAX1039 (AIN0) is 5V per amp of current out of the peak power tracker.

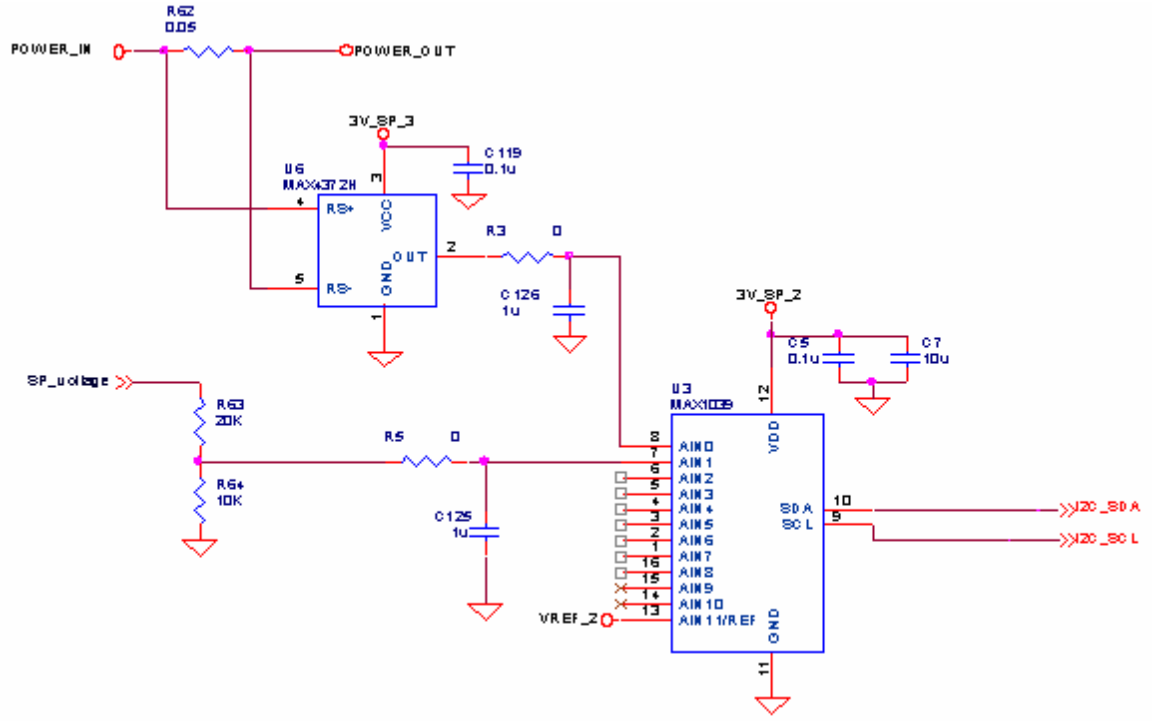

Figure 9. Voltage and current sensing circuit.

The current sensed will be between 0 and 350mA. This gives a voltage range of 0 to 1.75V into the ADC. The ADC is a MAX1039 that runs at 3V, has an internal 2.048V

reference, reads up to 12 analog channels at 8 bits of resolution, and interfaces to an 2-wire I^2C bus. The input voltage range utilized is 87.5% of the ADC's usable input range. The resolution achieved at the ADC is 1.6mA per step from equation 1.

Resolution=Vref/2^8*(current to ADC input ratio) (equ. 2)

Resolution=2.048V/255*1A/5V≈1.61mA

This resolution should be adequate for current sensing as there are more than 200 steps from minimum to maximum current. Equation 3 defines the number of usable steps in a data acquisition system.

# of steps = int((Maximum value)/(Resolution)) (equ. 3)

217 steps = int(350mA/1.61mA)

Before the signal reaches the ADC, it goes through a low pass filter created by R3 and C126. With R3=0Ω, the low pass filtering is minimal. Future testing will determine how much filtering is needed. To adjust the filter, R3 and/or C126 can later be replaced with similar devices with various values.

With the current sense resistor on the positive side of the MPPT output, the current is sensed using a circuit known as a high side current sensor. While low side current sensing has the advantage of requiring only a single ended analog voltage (referenced to

ground), it also can induce inaccuracies. Low side current sensing is less accurate than high side current sensing because resistance in the ground path changes the effective resistance of the sense resistor. Low side current sensing can also cause trouble when sending data to another circuit that isn't using the low side current sensor. The data sent by the circuit with the low side current sensor has its signals' voltage shifted above ground by a value equal to the voltage across the current sense resistor. For example, if a low side current sense resistor has 0.3V across it and an analog voltage of 1.2V is transmitted from the sensed circuit to another circuit, the voltage received will be 1.5V.

The advantage of low side current sensing is that it is possible to simply send the single ended voltage to a single ADC channel and have the current measured with little or no additional circuitry. When voltage amplification is required, the amplifier does not have a large common mode voltage to cope with as a high side current sense amplifier does.

A disadvantage of high side current sensing is that it requires a high common mode rejection (CMR) in the current sense amplifier. The MAX4372 is a current sense amplifier that is designed to accurately sense current with a low circuit component count. It is designed with an 85 dB CMR which attenuates the common mode error to less than 1uV in our application. The MAX4372 will amplify the voltage difference across a current sense resistor and output a single ended voltage without high precision gain setting resistors or any other passive devices.

One common disadvantage between high and low side current sensing is that the energy lost across and the voltage drop of the current sense resistor may be significant. The voltage drop of this circuit is kept minimal because the current sense resistor is only 0.05 ohms. This leads to a maximum voltage drop at 350mA of only 17.5mV. The 17.5mV drop is only 0.5% of the minimum system operating battery voltage of 3.4V and should be insignificant. The power loss is also minimal as the I^2R losses come out to a maximum of 6.1mW.

The voltage of the solar panel is sensed using a simple voltage divider. The input to the voltage divider is 0 to 4.4V and the output must be between 0 and 2V. For simplicity, the voltage is divided by an integer value to keep the scaling factor simple in hand calculations and in software. R63 and R64 are 20kΩ and 10kΩ, respectively. This ratio divides the input voltage by 3 and gives a maximum voltage into AIN1 of 1.47V. Therefore, the output voltage range will be 0 to 1.47V. This circuit gives a resolution of 24.1mV using equation 4. The number of ADC steps used is 183 through equation 3.

Resolution of voltage sensor = Vref/1^8*(sensor voltage to ADC voltage ratio) (equ. 4)

2.4.3 C&DH Processing

The ADC values for voltage and current are sent to the C&DH processor so that the Power Point Tracking software can maximize the output power of each solar panel. The processor multiplies the voltage and current values and creates a value of power. Maximizing the power value is the goal of the software.

After the power value is determined, it is compared with the previous power value. If the previous power value is less than the current power value, the change in digipot setting between the last power reading and the current power reading was a change toward the MPP. In this case, the digipot setting is incremented in the same direction as it was last time. If the current power value is less than the previous power value, then the digipot was incremented in the wrong direction and the digipot is incremented in the opposite direction as it was previously.

The effect of this system is that it "hunts" for the peak power by constantly adjusting the solar panel voltage set point by small amounts through digipot adjustments. This simple feedback system does not require the software to know the actual number of watts being produced or the actual solar panel voltage set point; the software only requires a value proportional to the power level and a digipot value that it can use to change the solar panel voltage set point. Because the processor doesn't know the absolute values of its input or output values, this feedback system can be adapted with little or no modification to other solar power systems.

2.4.4 Individual MPPT or Summed MPPT

Now that the design has been selected, a decision needs to be made as to whether to peak power track each solar panel side individually or all together. If they are tracked individually, only one peak power tracker will be needed and if individual peak power tracking is used, the solar panels will be used more efficiently.

If we PPT all of the solar panels together, the electronics design will be simpler, lighter and consume less space. This conservation, though, would come at a price. Each solar panel will have a different amount of incident light and temperature. These differences will give each solar panel a different peak power point and operating the panels together would not allow them to operate at their most efficient voltage. Although PPT all solar panels together is less efficient than PPT for each panel, it is more efficient than not implementing PPT at all.

If PPT is implemented for each individual solar panel, the energy efficiency would be greatest but the mass and volume taken by the peak power trackers would be several times greater. To allow individual PPT we will need extra circuit board space. CP2 is designed with circuit boards as its sides that allow the solar panels on the outside of the circuit board and electronics on the inside. The inside of the PCB provides an excellent place for the MPPT electronics and because this MPPT circuit uses few components, it does not take up a substantial amount of circuit board space and consumes very little mass. Since providing MPPT to every solar panel is feasible and does not consume much volume or mass, we decided to utilize it.

2.4.5 Limitations

There are some limitations on this design. The circuit does not MPPT when the C&DH processor isn't operating since the processor is needed to shift the solar panel voltage set

point. Also, the solar panel voltage must be at or above the battery voltage for MPPT to take place.

Under the condition where CP2's batteries are discharged, the PPT system will not turn on as it requires a regulated 3V supply for its digital logic. With the batteries discharged, the PPT system will not turn on and allow solar panel power to charge the batteries or power the satellite. To initially charge the batteries and turn the satellite "on," a silicon diode is used to bypass the PPT when the solar panel to battery voltage difference is above 0.7V. This allows the solar panel to charge the battery past a minimum voltage and the satellite electronics will engage. The battery voltage required for the power system to turn on the satellite is 3.4V. This voltage is easily achievable with a 4.4V solar panel and a 0.7V diode voltage drop.

The disadvantage of this form of bootstrapping is that the silicon diode consumes a fair amount of power and does not charge the battery very efficiently. This disadvantage is not critical because the diode will only be on and consuming power during a short time while the battery is being charged to 3.4V. The amount of charge that the batteries will require to reach 3.4V is about 50mAh, which a solar panel can supply in about 12 minutes. Once the batteries reach 3.4V, the power system will engage the C&DH processor and the 3V supply for the side panels' digital logic. The MPPT system will turn on and bring the solar panels to the optimal operating point.

In the condition of a C&DH processor failure, whether from a single event upset or a failure in software, the PPT must operate to some minimal level in order for the contingency mode to function properly. In contingency mode, the C&DH processor is bypassed and the payload works directly with the communications system to downlink payload data and successfully complete the mission. The worst-case situation that must be considered is where the C&DH processor sets the PPT to the voltage set point so high that the solar panel never reaches it and the MPPT never turns on. Under this condition, the silicon diode will bypass the MPPT and charge the battery to a minimal level. At this minimal voltage, the batteries will reach a voltage somewhere between 3.5V to 3.7V and will be charged to 0.7Wh and 1.1Wh. Giving the satellite enough energy to operate and complete its mission. Thus, an errant C&DH processor will be unable to fully sabotage the satellite and prevent the solar panels from producing any electricity.

It should be noted that the peak power voltage of the solar panel is 4.17V at 28 deg C. Charging the batteries to 4.2V usually will require operating the solar panels at a voltage above the maximum power voltage. This is because the MPPT design utilizes a Buck DC-DC converter which can only lower the solar panel voltage. Operating at a solar panel voltage less than maximum is not a big disadvantage when the battery is at 4.2V. Once the battery is at 4.2V, it is mostly charged and the need for maximum power from the solar panels is lower than when the battery is mostly discharged.

2.4.6 Results

The design of this MPPT allows a test bed for CP2 and future satellite MPPT designs to maximize the power produced by a solar panel design. Utilizing MPPT allows the solar panels to produce power efficiently and changes the solar panel voltage to the battery voltage, thus saving another DC-DC converter. The method of MPPT presented here is a compact version that does not require full microcontroller supervision or more than 2 I/O pins and allows the microcontroller to perform other tasks while peak power tracking.

The MPPT circuit has been built into a small section of the back of CP2's side panels. The circuit shown in Figure 10 is the MPPT circuit after conformal coating.

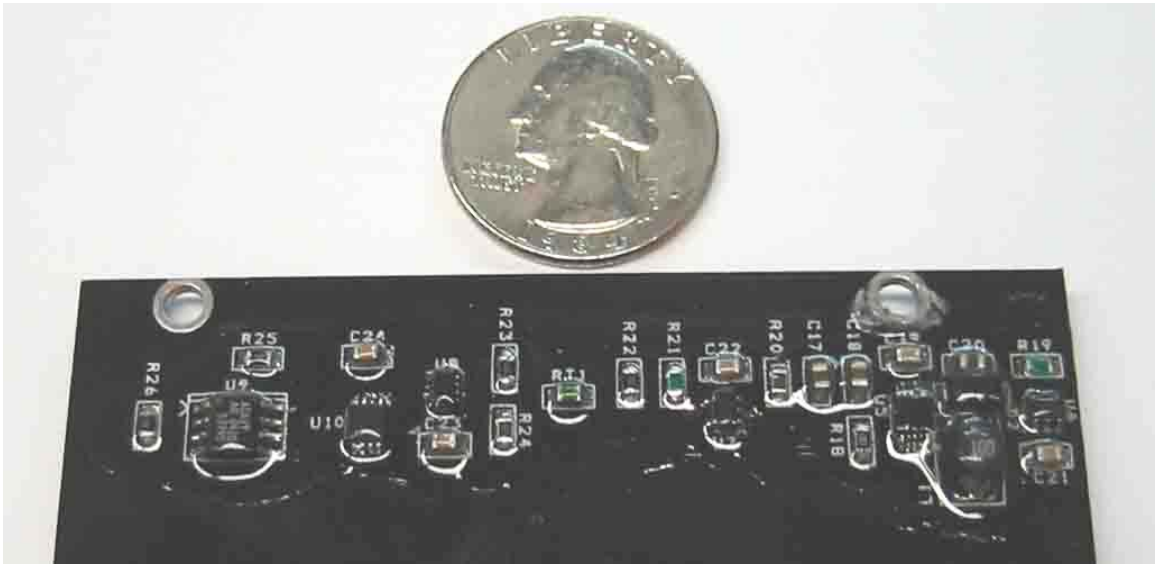

Figure 10. MPPT circuit on side panel.

The MPPT system is presently under testing. The voltage and current as a function of digipot settings during testing are shown in Figures 11 and 12.

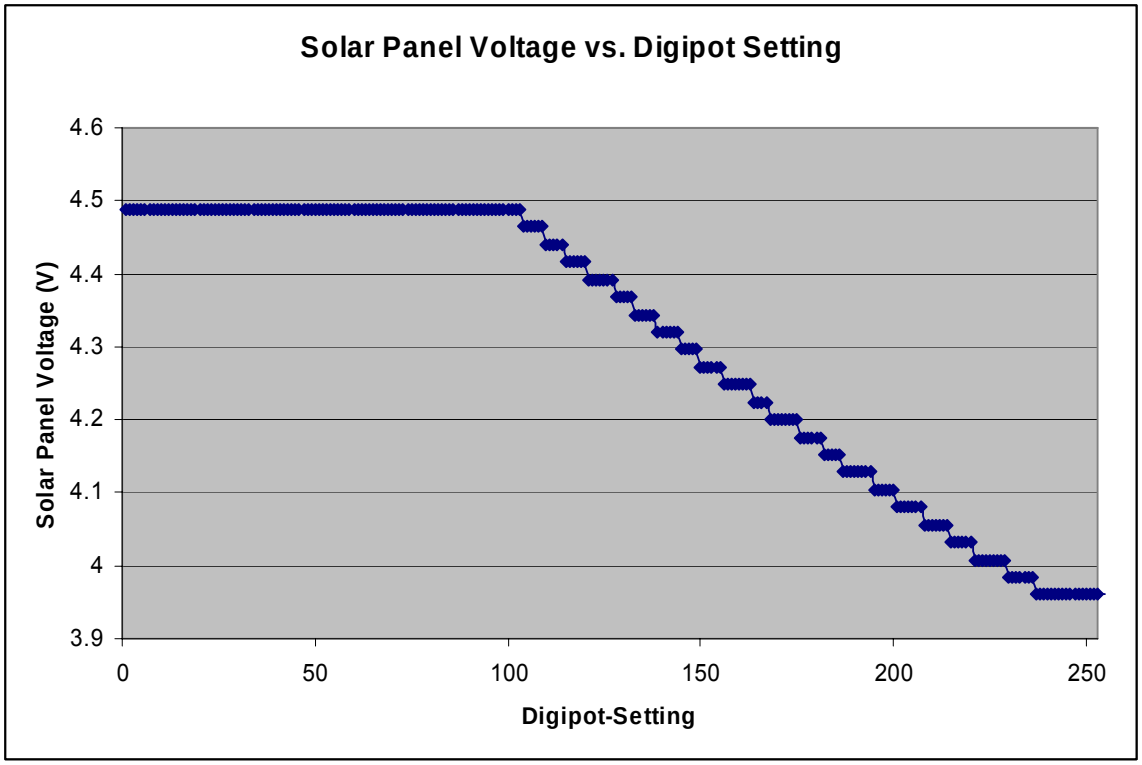

Figure 11. Solar Panel Voltage Versus Digipot Setting.

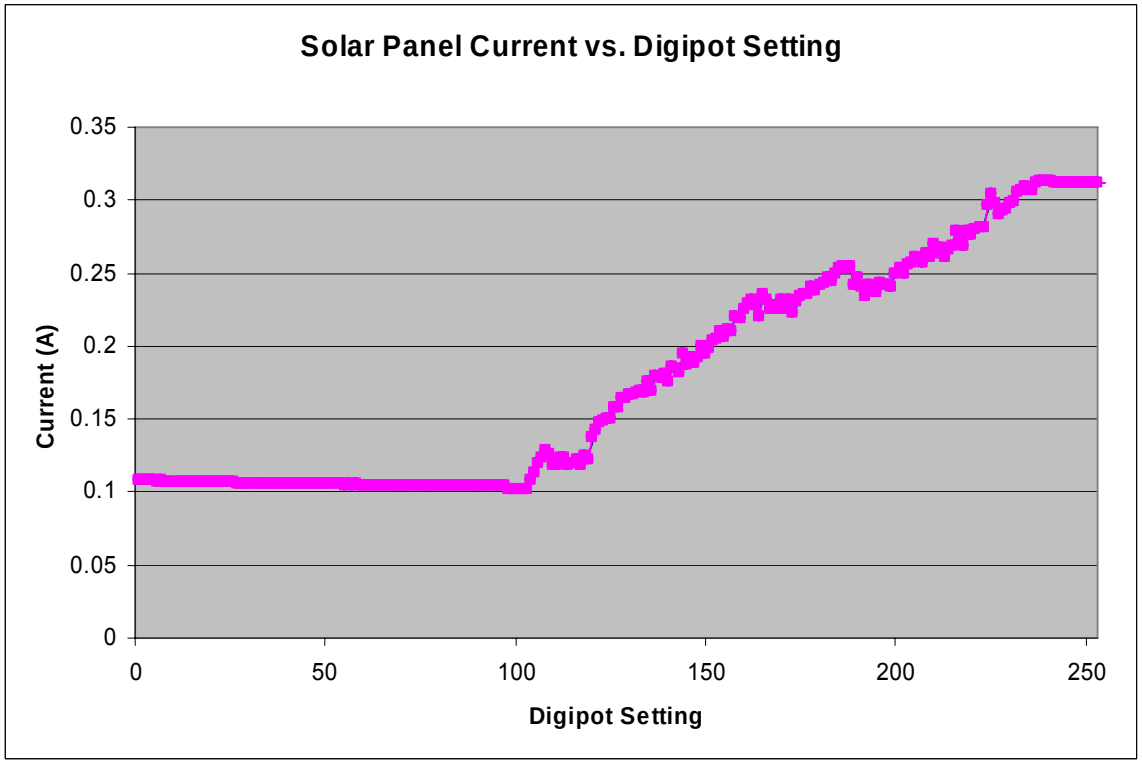

Figure 12. Solar Panel Current Versus Digipot Setting.

2.5 Energy Storage, Battery Protection, and Battery Data Acquisition

2.5.1 Energy Requirements and Battery Selection

The energy flow into CP2 will unfortunately be both cyclical and small. The orbit that CP2 will be launched into gives an approximately 90 minute cycle with about 60 minutes of sunlight and about 30 minutes of darkness. Thus, batteries must store energy for the 30 minutes when the solar panels will not be operating. When CP2 is in sunlight, the solar panels should provide between 1W and 2W of power. This power input level is inadequate during radio transmissions as the transmitter consumes around 3W of power. This means that during any time when the satellite is transmitting data to earth, power will be required from the batteries whether or not the solar panels are producing energy.

The battery circuit for CP2 must hold enough energy for 15 minutes of transmission and 30 minutes of darkness. This transmission time is chosen because it is the length of time that the satellite will be in view of a ground station during an optimal pass. The amount of power required during darkness while not transmitting is very small, about 150mW.

At this point in time, it is appropriate to question the energy storage required for the payload. This is difficult to estimate and, since CP2 is designed as a multi-payload bus, there is no specific answer. We have therefore determined that we will store as large of an amount of energy as is reasonable based on battery size, volume, and mounting constraints. By doing this, we will attempt to provide an adequate energy supply to as

wide a variety of payloads as possible. If a payload requires more energy storage than the CP2 bus provides, the payload can carry its own energy storage devices such as batteries or ultracapacitors.

CP2 will also be designed to carry extra energy capacity for a few reasons. First of all, the extra energy capacity allows CP2 to have a shallow depth of discharge (DOD) that promotes longer battery life. This is discussed more thoroughly in the next section. Secondly, the extra energy can be used to allow the RF communications system to download pieces of a large data file to multiple ground stations in rapid succession. This means that, rather than waiting for several satellite passes over one ground station for a few days, data can be downloaded to several ground stations across the world much more quickly.

Extra energy storage is also needed in order to simplify the electronics system. Previous CubeSat designs involved using a heating element and a thermostat to regulate battery temperature. The disadvantage of this design is that if the control system fails with the heaters on, excessive power dissipation will lead to satellite failure.

In CP2, the thermal team and electronics team decided on using two methods that allows us to move away from heaters. We thermally insulate the batteries from the structure and from the side panels. This has the effect of reducing the batteries' temperature extremes in the same way that a large pool of water stays cool in hot weather and yet never freezes in the winter. The other method we employ to prevent heater requirements is to have

excess energy storage. This compensates for the temporarily unavailable energy if the temperature of the batteries fall too low.

An example of the (temporarily) unusable energy inside a typical Li-ion battery at various temperatures is shown in figure 13. The top curve represents the maximum charge capacity and the two curves below it represent the battery charge state when the battery is considered discharged.[2]

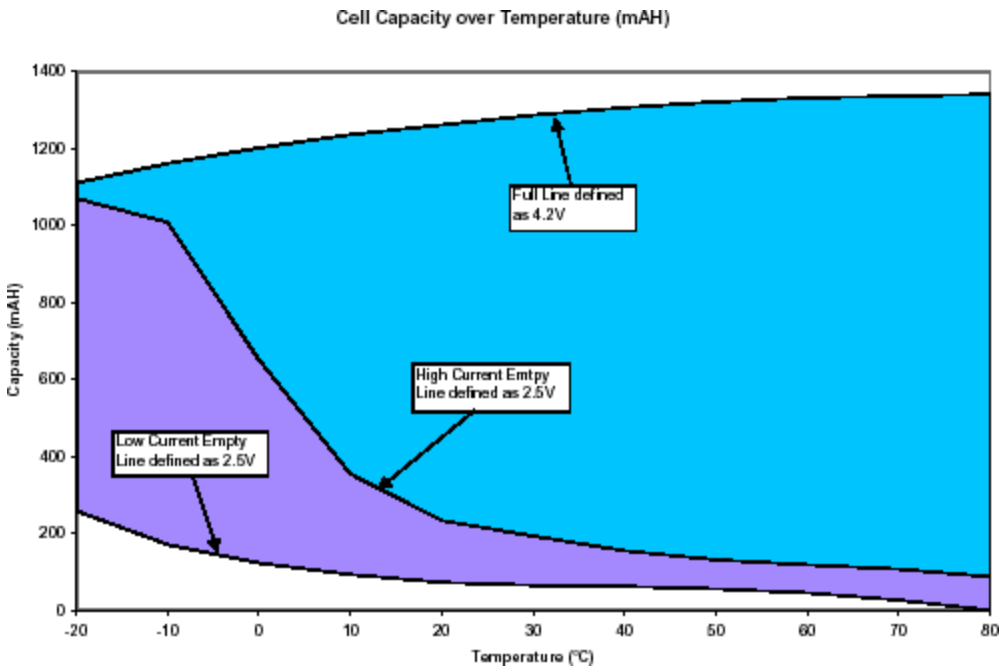

Figure 13. Battery capacity available at various temperatures and discharge rates.

In this figure, the battery capacity is represented by the vertical distance between the full line and the empty lines. For CP2, the discharge rate will be somewhere in between the high and low discharge rate lines. As the figure shows, the amount of available charge decreases rapidly as the battery temperature decreases below 0 deg C. This fact points to

the need for excess energy capacity for battery operation at low temperatures if a battery heater is not employed.

Another factor in battery selection for CP2 is Space Shuttle requirements. We designed CP2 for space shuttle compatibility so that future launches of CP2 could be made from the Space Shuttle. Unfortunately for the energy storage system, the Space Shuttle requirements do not allow Li-ion batteries of any sort.

The following points summarize the pertinent attributes of the battery chemistries during design time that are considered:

Ni-Cad:

- Advantages: Used and characterized for space applications. High power density.
- Disadvantages: Low energy density. Full cycling required to remove memory effects.

Ni-MH:

- Advantages: High energy density. Allowable on the Space Shuttle.
- Disadvantages: Lower energy density than Li-ion.

Li-ion:

- Advantages: Extremely high energy density. Medium power density.
- Disadvantages: Not allowable on the Space Shuttle.

Based on these requirements, the battery characterization of CP1's Li-ion batteries, and our design experience with CP1's Li-ion batteries, we found that the Ni-MH battery chemistry is the only one that met the requirements. However, it does not give us the high energy per volume and energy per mass values that we are looking for. We need Ni-MH batteries to meet CP2's mission requirements but prefer the high energy capacity of Li-ion cells like the ones used on CP1.

We decided to have an energy storage system that would accommodate Li-ion or Ni-MH battery packs in the same prismatic form factor. The Ni-MH battery pack would consist of 3 cells in series to give an operating voltage near the Li-ion battery. With this system, we can use Ni-MH batteries on a build of CP2 that will be flown on the Space Shuttle and we can use the Li-ion cells, with superior energy density, on all other flights.

The Li-ion batteries we choose are much like the Li-ion batteries chosen for CP1 except the capacity has been increased by 12.5%. They have 1350mAh of capacity in a size, have an operating voltage range from 3V-4.2V and have an average operating voltage of 3.7V.

For ease of interchangeability, we choose a Ni-MH pack form factor that is almost identical to the Li-ion battery form. The Ni-MH battery is a 3-cell pack from GP Batteries. With 3 cells, the Ni-MH pack has an operating voltage range from 3-3.9V, a

typical operating voltage of 3.6V, and a capacity of 700mAh. The Li-ion battery pack has approximately twice the energy of the Ni-MH battery pack even though the Ni-MH battery pack weighs 10g more.

2.5.2 Battery Failure Prevention and Failure Isolation

Batteries have a high rate of failure compared to other electronic components. Therefore we want to minimize the rate of battery failure and have adequate redundancy in order to maximize the useful life span of our energy storage system on CP2.

The life of a battery is greatly shortened as the Depth of Discharge (DOD) per cycle increases. Having a DOD of 20 to 40% extends the cycle life of a Li-ion cell significantly. This is important because the battery will be charged and discharged every orbit with approximately 480 orbits every month. This means that a year of operation will apply 5760 cycles to the battery. Although the life span of CP2 has been set at 3 months, we are designing the energy storage system for a lifespan of at least one year. This means that the batteries must withstand about 5760 cycles before battery capacity is lost due to excessive use.

The shelf life of our batteries should not become a factor in the battery failure analysis unless CP2 is shelved for a few years. Therefore, the batteries must have a shelf life of at least 3 years, preferably more. Three years is an adequate time for the batteries to be stored, built into the spacecraft, stored in CP2, and flown. The self discharge rate of the

chosen batteries need not be a critical consideration as CP2 is designed to operate even if the batteries begin in a discharged state. Also, 3 months before launch we will be allowed access to CP2 (through the umbilical connection) and can top off the batteries at that time.

Even with light DODs and youthful batteries, a battery failure could mean the end of a mission if the energy storage circuit does not prevent failures and have redundant batteries. The battery protection circuit discussed in the next section prevents battery failures from causing a complete failure of CP2's power system. But we must also have redundancy in the batteries (and battery protection circuits) in order to keep energy storage in the event of a battery failure. For this reason, CP2 is designed with two battery packs and an individual battery protection circuit for each battery.

2.5.3 Battery Protection Circuit Requirements

The battery protection circuit must not only protect the batteries from damage but it also must protect a battery short from shorting CP2's main power bus. The battery protection circuit should prevent several different battery damaging conditions:

- Battery over voltage (overcharge)
- Battery under voltage (overdischarge)
- Battery overdischarge current (short circuit on CP2 bus)

- Battery overcharge current (short circuit in battery)

Battery Over Voltage (Overcharge) The batteries on CP2 must be prevented from overcharging. The battery over voltage condition will occur on Li-ion batteries that are overcharged or charged with too much current when they are almost fully charged. The over voltage condition, usually around 4.2V, can be sensed by the battery protection circuit which can then remove the charging current from the battery. Ni-MH batteries, though, do not exhibit an over voltage condition when they are overcharged. They need another method of end-of-charge determination. The common end-of-charge determination methods for Ni-MH are zero dV/dt, negative dV/dt, dT/dt, and timer control. To prevent overcharging of CP2's batteries, we must use a battery protection circuit that will prevent either Li-ion batteries or Ni-MH batteries from over charging. Protecting Li-ion batteries is straight forward, but protecting Ni-MH batteries is more complex.

The zero dV/dt and negative dV/dt end of charge methods monitor the change in battery voltage during charging and end the charge when the battery voltage stops increasing or begins decreasing. This method of charge termination is designed for constant current (CC) charging and will not work well on this power system that does not employ CC charging. The batteries' charge current will vary with time as the solar panels provide more or less power and as the satellite performs its normal routine. With varying charge current, the battery voltage will also vary, giving zero or negative dV/dt signals before charging is complete.

The dT/dt method of charge control detects the increase in battery temperature that occurs around the time when the battery is fully charged. This method of charge control will not work on CP2 because battery temperature will fluctuate with the sunlight/darkness cycle of the satellite's orbit. This fluctuation means that the dT/dt method may give false readings of charge state before charging is complete. The batteries may also be charged slowly and they could produce little heat when they are overcharged, thus causing an undetected overcharge condition.

The timer method simply shuts off the charging circuit after a predetermined charge time. This method, like others, requires a CC charging circuit. It, therefore, will not work for our application.

A method not usually used as the primary method for end of charge detection is coulomb counting. It is usually not used since it is more complex than the other methods and can be less accurate when not maintained properly. The coulomb counter monitors the coulomb count into and out of the battery and the balance is the number of coulombs of charge inside of the battery. The system works much like a bank account. The amount of money in a bank account can be determined if we know the initial funds in the account and then simply add the value of every deposit and subtract the value of every withdrawal. By keeping track of the flow of money going in to and out of the bank account, we don’t have to check the balance; we always know what it is.

A coulomb counter works the same way by monitoring the current flow into and out of the battery. It too has to be reset to a known value. This is usually done with a fully charged or fully discharged battery. The coulomb counter then can tell the C&DH processor the charge state of the battery. If the battery is at a fully charged state, MPPT could be shut off so that less power would be produced by the power system or, better yet, useful systems could be turned on more frequently. For example, more radio beacons could be sent to earth or the payload could be turned on more often. Using a coulomb counter to detect end-of-charge is useful in our case because it works with either Li-ion or Ni-MH batteries and no additional components are required to control battery charging.

Battery Under Voltage (Overdischarge) The under voltage condition is not as much of a problem with Ni-MH batteries as it is with Li-ion batteries. Li-ion batteries can be permanently damaged if their voltage drops too low, usually around 2.6V-3V. Ni-MH batteries can be discharged and left with their terminals shorted together without permanent damage. The battery protection circuit must detect the low voltage condition and prevent the battery from being excessively discharged.

Battery Overdischarge Current (Short Circuit on CP2 Bus) The battery current must be monitored for excessive discharge current. If the discharge current is too high, the load should be disconnected after a fraction of a second to prevent battery damage. The battery should not be disconnected too quickly, because a starting load could draw

excessive current for a brief period of time. This surge in current should not cause the battery to be disconnected. On the other hand, if a sustained short circuit condition occurs, the battery should be disconnected as soon as possible.

Battery Overcharge Current (Short Circuit in Battery) In addition to excessive battery voltage during charging, another damaging factor is excessive charge current. At first glance, the charge current is inherently limited because the solar panels cannot produce very much current. A charging battery cannot be charged from the solar panel with excessive current because even with optimal solar irradiance on 3 solar panels, the maximum charging current with a battery voltage of 3V is about 650mA, well below the 2A maximum charge current that the battery is designed for. Because of user error, however, the batteries could be charged with excessive current from the satellite's umbilical connection, causing damage. A condition could also occur where the battery voltages are different from one another and one battery might be charging the other battery at excessively high currents. To protect the batteries from these conditions, overcharge current protection is required.

2.5.4 Battery Protection Circuit Design

The battery protection circuit is shown in Figure 14. The heart of the circuit is the DS2761. In addition to the protection requirements listed above, the DS2761 also provides the following features:

- Zero voltage battery recovery charge
- 32B of EEPROM for battery characterization

- Single wire communications bus
- A battery data acquisition system that collects:
    - ♦ Battery voltage
    - ♦ Battery current
    - ♦ Accumulated battery current
    - ♦ Battery temperature
    - ♦ Protection circuit state

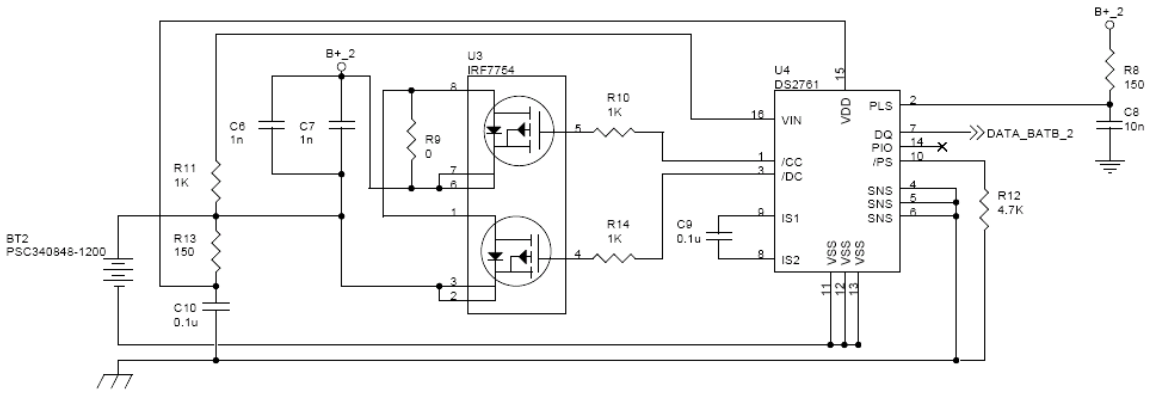

Figure 14. Battery Protection Circuit.

With the data acquisition system embedded into the DS2761, the battery protection and sensory system only requires two ICs per battery. The second IC is the IRF7754, a dual P-channel MOSFET. The DS2761 pulls the gate of one P-channel MOSFET high to disable discharging and it pulls the other gate high to disable charging.

In this circuit, the positive terminal of the battery connects to the main CP2 power bus, B+, through two "back to back" P-channel MOSFETS. This means that one MOSFET

can block current in one direction and the other MOSFET can block current in the other direction. The negative terminal of the battery is connected to VSS pins on the DS2761. VSS pins are connected to SNS pins internal to the DS2761 by an internal 25mΩ current sense resistor. SNS is connected to a "battery ground" that is connected to satellite ground after a series of switches. The switches are the redundant Remove-Before-Flight (RBF) switches and deployment switches used to turn on the satellite. In order to attach the negative terminal of the battery to ground and activate CP2, a RBF switch and a deployment switch must activate. The RFB will be removed after CP2 has been installed in the P-POD (Poly Pico-satellite orbital deployer).

In addition to this main path for battery power in Figure 14, there is also a pair of low pass filters for the DS2761 to determine battery and bus voltages. R6 and C5 are used to detect the battery voltage and will filter out any noise or voltage sags on the battery voltage. R1 and C3 are used to detect the voltage on B+ and filters out noise and voltage sags on B+. With the DS2761 sensing the battery voltage, B+ voltage, and battery current flow, all potential hazard conditions can be detected and prevented before battery damage can occur.

2.5.5 Battery Protection Operation

Overdischarge Current When the DS2761 senses an overdischarge current condition of about 1.8A for more than approximately 10ms, the battery discharge path is disconnected. High surge currents of several amps are allowed for up to 5ms The DS2761 shuts off the discharge control MOSFET by pulling U1 pin 4 high. This shuts off the MOSFET and the body diode of the discharge control MOSFET prevents further discharge. The battery is effectively disconnected from the load and it will not be damaged from the heavy drain.

If both battery protection devices detect an overdischarge current, the load will cause CP2 to power down its systems, as the solar panels will definitely not be able to supply a load current that the batteries cannot. At this point, if the excessive load on the bus is a permanent failure, the power system cannot recover. If, on the other hand, the high current consumption is temporary, the power bus will power up again as soon as the fault condition has subsided and a solar panel receives light. When the solar panel supplies power to CP2's main power bus, the batteries will reconnect to the bus when the bus voltage increases above 1V less than the battery voltage. As the bus voltage rises and the batteries reconnect, the power system will regain full functionality.

In the case when the batteries connect to the bus at different times and, hence, will both be connected to the bus with approximately a 1V difference between battery voltages, a problem could occur. With two battery voltages 1V apart, the higher voltage battery

could try to charge the other with such high current that the battery safety circuit on one of them could trip and disconnect a battery. Testing has shown that with battery voltages 1V apart, the batteries' currents do not exceed the charge or discharge current limit of the battery protection circuit.

In operation, the battery is separated from the load in about 10ms. This is shown by the battery voltage in Figure 15 where the battery load is disconnected in 11ms.

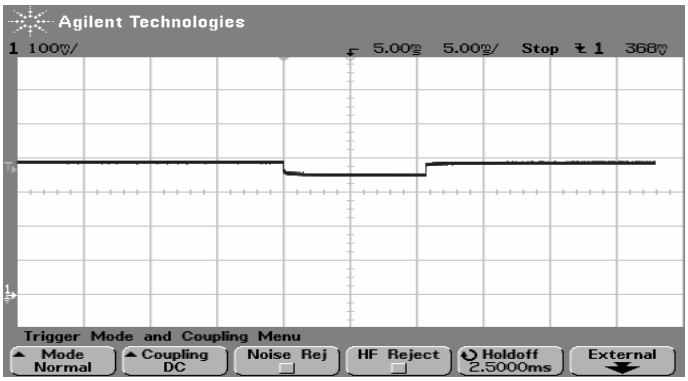

Figure 15. Battery Voltage During Overdischarge Current Condition.

Overcharge Current If the DS2761 senses an overcharge current above about 1.8A for more than about 10ms, the discharge control MOSFET will be shut off as the DS2761 pulls U1 pin 4 high and the discharge control MOSFET's body diode will prevent any further charge current from flowing. This situation will not occur during normal operation and the correction for it is to lower the main power bus voltage below 1V below the protected battery voltage. If the situation is one where a battery has shorted and has received too much "charge current", then the battery will stay disconnected as it should be.

Short Circuit Under a short circuit condition, the battery discharge path is shut off within 120us. The discharge circuit is broken in the same way as in the overdischarge current case. Other than the quicker disconnection than the overdischarge condition, the effects and ramifications of a short circuit are identical to the overdischarge condition.

In operation, a short circuit only affects the battery for about 100us. An example of this is the battery voltage shown in Figure 16 indicating that the short circuit is disconnected within 120us.

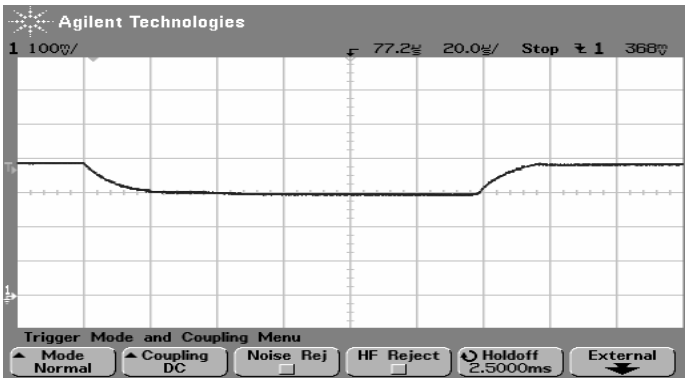

Figure 16. Battery Voltage During Short Circuit Condition.

Over Voltage The over-voltage condition will occur when the batteries are nearly charged and the solar panels supply more power to the CP2 main power bus than the loads require. Under this condition, the DS2761 disconnects the batteries from the main power bus and reconnects it a short time later after the battery voltage has dropped to a slightly lower level. The over voltage protection activates at about 4.275V and deactivates at about 4.15V. This means that during the last portion of the battery charge

cycle, the battery will be repeatedly connected to, and disconnected from, the main power bus. As the batteries reach full charge, the duty cycle over which they will be disconnected from the main power bus will become greater until they are rarely attached.

A special problem occurs when Ni-MH battery packs are charged using this charging system. The 3-cell Ni-MH battery pack chosen for CP2, has a discharge voltage similar to the Li-ion battery pack, between 3.3V and 3.75V. However, the Ni-MH pack voltage during charge can be significantly higher than the Li-ion cells chosen for CP2. The Ni-MH battery pack charges at between 4.2V and 5.2V. This means that if the Ni-MH pack is used on CP2 and the batteries are charging, the DS2761 will consider the normal charging voltage to be too high and disconnect the charging circuit.

Our solution is to bypass the DS2761 discharge control MOSFET and use other means to control the charging of the batteries. With the DS2761 battery discharge control disabled, the C&DH processor will be used to prevent overcharging. The C&DH processor has two options to prevent overcharge. One is to disable peak power tracking. With this option, the processor changes the solar panel voltage set point so that it produces an intentional sub-optimal power level. Reducing the solar power to equal the load power consumption will prevent an over charging of the battery. The second solution is to increase the power consumption of the loads on CP2. For example, the radio beacon could be sent more often or the payload may be activated more often. Using this method, the satellite can become more active and it is, therefore, the preferable option.

At this point it is appropriate to note that the range of MPPT output voltages supplied to the main power bus and the batteries reaches a maximum of about 4.2V to 4.3V due to the Buck DC-DC converter topology used in the MPPT circuit. With a maximum MPPT voltage at the low end of the Ni-MH battery pack charging voltage, the Ni-MH batteries may not charge at an optimal rate. A solution would be to use a Buck-Boost or a SEPIC DC-DC converter in the MPPT circuit. This has not been implemented as Space Shuttle launches (requiring Ni-MH use) for CP2 have become highly unlikely since the beginning of the CP2 design process.

Under Voltage In the case where the batteries are nearly depleted and the main power bus continues to discharge the batteries, the DS2761 will break the discharge current path and prevent the battery voltage from decreasing below safe levels. Li-ion batteries can be permanently damaged if their voltage is reduced below about 2V. This under voltage disconnect cannot operate during normal satellite operation, though, because the loads will shut down if the battery voltage decreases to 3.08V. For more information on the load shut down circuit, see the Load Power Conditioning section.

2.6 Power Distribution

CP2's power system must supply power to electrical loads, often at a regulated voltage, and reasonably isolate the loads so that an open or a short circuit at one load effects the other loads minimally. A balance must be met, though, where the complexity of circuit

isolation and circuit complexity meet. Figure 17 indicates the load power distribution system that has been designed for CP2.

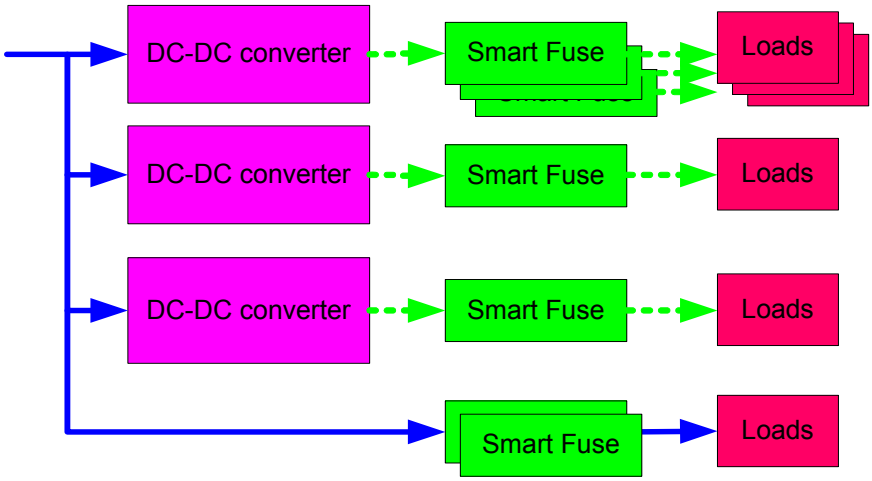

Figure 17. The load power distribution system on CP2 is designed with separate DC-DC converters on each major load power branch and smart fuses on each small load branch. CP2 is designed so that a failure of any one DC-DC converter will not cause a mission failure.

The power distribution system is designed with five major power branches. Three of the major power branches use DC-DC converters to convert the unregulated battery voltage to a regulated 3V supply. The other two branches operate with the raw battery voltage.

2.6.1 DC-DC Converter Circuit

A DC-DC converter circuit designed for CP2 is shown in Figure 18. Because all loads requiring regulated voltage operate with 3V, the three DC-DC converter circuits are identical. They each include a low voltage cutoff that removes power if the main power

bus voltage drops to extremely low levels, a highly integrated and low part count DC-DC Buck converter, and a temperature sensing circuit.

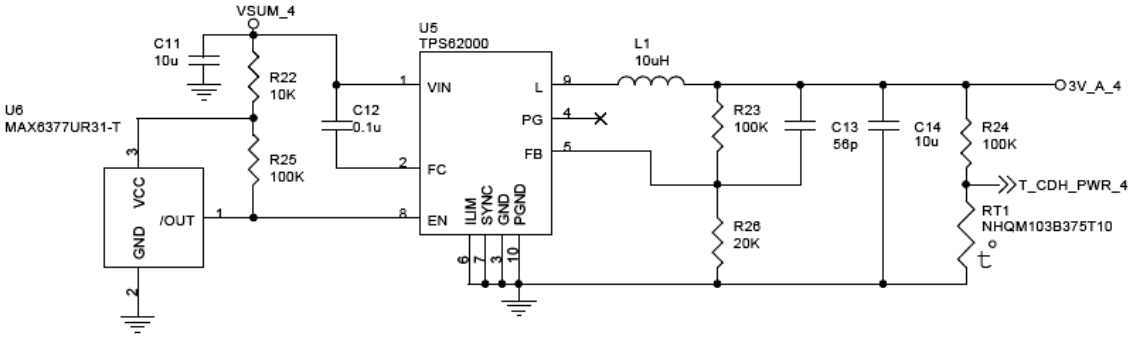

Figure 18. This DC-DC converter circuit includes a low voltage cutoff with hysteresis, a DC-DC Buck converter, and a temperature sensor.

DC-DC Converter IC U5, the TPS62000, is a synchronous step-down DC-DC converter with integrated MOSFETs designed by Texas Instruments. The device is rated for an input voltage range from 2-5.5V which is more than adequate for our requirements. Unfortunately, the output voltage of 3V is not one of the fixed output voltages that this family of ICs offers. As an alternative, we use two fixed external resistors to set the output voltage. This device has several major advantages:

- Input voltage range is within Li-ion battery operating voltage range
- Output voltage can be set to 3V
- 100% maximum duty cycle for low drop out voltage
- Current limit at 600mA to prevent direct short circuit
- Pulse Frequency Modulation (PFM) mode used at light loads to increase efficiency

- Synchronous rectification for efficiencies up to 95%
- Integrated N and P channel power MOSFETs for low circuit part count
- 50uA typical operating current
- Tiny 10 pin MSOP package
- 750kHz typical operating frequency in PWM mode reduces inductor and capacitor size requirements

By using this device, physically small capacitors and inductors can be selected to complete the DC-DC converter circuit.

Texas Instruments suggests a 10uF capacitor as the DC-DC converter input filter.[3] Since such a small capacitance is required, only a tiny 0805 size capacitor is used as the input filter to reduce the footprint of the DC-DC converter circuit.

The inductor selected is a shielded 10uH from Tyco Electronics. With such high integration densities, I looked for shielded power inductors to reduce noise coupling to other components on the satellite. The inductor has a saturation current of 1A, a DC resistance of 0.075Ω, and consumes less than $0.3cm^2$ of board real estate. The maximum current through the inductor can be determined by the following equations:

$$\text{delta } I_l = Vo*(1-Vo/Vi)/(L*F) \qquad \text{(equ. 5)}$$

$$I_{l(max)} = I_o + \text{delta } I_l/2 \qquad \text{(equ. 6)}$$

The maximum output current from any of the DC-DC converters is 450mA. In reality, only the DC-DC converter powering the C&DH (Command and Data Handling) system and the side panels will have a maximum current of 450mA but making identical circuits will simplify design, testing, and population.

Delta I1 = 3*(1-3/4.5)/(10u*750k) = 133mA

I1(max) = 0.45 + 0.133 = 583mA

With a maximum current of 583mA, the DS6630-100M is selected with a maximum current of 1A. The series resistance of this inductor is 0.075Ω. With this series resistance, the current loss, even with 450mA of current flow, is only 15mW.

The output capacitance, like the input capacitance, can be 10uF as per the TPS62000 design guide's suggestion. Because the input and output capacitors are the same, both capacitors are of the same type.

Low Power Cutoff U6, R22, and R25 together create a simple low voltage disconnect with hysteresis. A MAX6377UR31-T precision voltage detector, U6, is normally used to keep a processor in reset during power up and brown out conditions (The PIC processors on CP2 have this built in). In this circuit, U6 is used to shut off the DC-DC converter

when the main power bus voltage is too low. If the voltage at U6's Vcc pin drops below 3.08V, the /OUT pin is pulled low with an open collector output.

During normal operation, /OUT is de-asserted and U6 pin 1 floats to the main power bus voltage. This condition keeps U5 pin 8 high and the DC-DC converter enabled. Under these conditions, the current through R22 is negligible and the voltage on U6 pin 3 is very close to the main power bus voltage. If CP2's batteries ever discharge enough that the main power bus voltage decreases to about 3.08V, U6 pin 1 will pull to ground and disable the DC-DC converter. Pulling the pin to ground will also turn R22 and R25 into a voltage divider. This voltage is "seen" by U6, pin 3 as the main power bus voltage divided by about 1.1. Under this condition, the main power bus voltage must rise to about 3.4V, not 3.08V, before U6 de-asserts /OUT and re-enables U5.

This hysteresis is critical to proper operation of CP2 due to battery voltage (generally equal to the main power bus voltage) variations in response to changing loads. Namely, if a battery's load is removed, the battery voltage increases. Without R22 and R25 providing hysteresis, the DC-DC converter enable line would oscillate during a low battery voltage condition. This circuit is shown in Figure 19. When the battery voltage is low enough for U6 to disable U5, the load would be disconnected from the battery and the battery voltage would rise. The battery voltage then rises above the internal high voltage set point of U5 (about 6.3mV above the low voltage set point). U5 would then sense the increased battery voltage and re-enable U6. With U6 enabled, the load is re-attached to the battery, the battery voltage drops below the internal voltage set point of

U5, and U6 is again disabled. This process can repeat itself and consume power while not allowing the systems on board CP2 to operate properly.

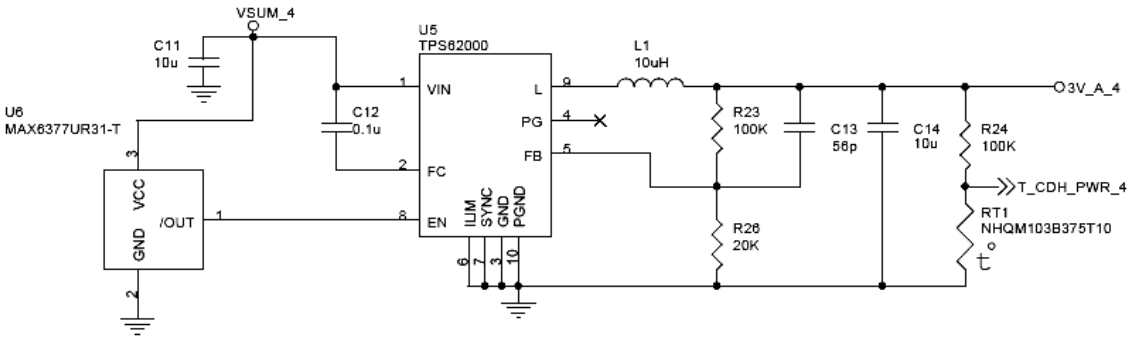

Figure 19. This circuit is much like Figure 18 except that R22 and R25 have been removed. Load power oscillation can occur due to this circuit.

With the low voltage set point set at 3.08V, the battery is allowed to discharge to between 96% and 98% Depth of Discharge (DOD). Discharging the batteries to this DOD repeatedly will reduce the cycle life of the batteries and should be avoided. Algorithms in software can reduce the overall satellite load when the batteries are partially discharged to prevent a 96% DOD. The satellite can transmit radio beacons less frequently or deactivate the payload temporarily in order to reduce battery DOD.

With the re-enable voltage set point set to 3.4V, the batteries will have to recharge by a small amount before the loads will be re-enabled. The batteries will be at approximately 95% DOD when the loads are re-enabled, assuming that the solar panels are not supplying power to charge the batteries and power the loads.

During normal operation, the ~97% DOD turn off and ~95% DOD turn on points have been calculated assuming there is no solar power input and the loads are in their normal, low power, state. If a higher load such as the RF amplifier or magnetorquer is activated with a mostly discharged battery, the battery voltage may drop too low and the loads will disconnect. After the disconnection, the battery voltage will quickly rise above 3.4V and the loads will be turned on once again. This quick power loss represents a situation where an oscillation will occur if the microcontrollers turn on heavy loads again soon after power-up. Because of this, when the microcontrollers are first powered up, they should default to disable magnetorquer operation and not immediately activate the RF amplifier.

If the batteries remain in a low charge state, it is possible for CP2 to send an RF beacon, cause the battery voltage to drop too low, and shut off power momentarily to the satellite loads. This condition represents a form of oscillation that should be avoided. To solve this problem, software can be used to reduce the RF amplifier output power and thus reduce its electrical power requirement.

Temperature Sensor The temperature of the DC-DC converter is important to the health of CP2. If the DC-DC converter becomes too hot or too cold it may not operate correctly. We therefore have a thermistor near each DC-DC converter to determine its temperature. The thermistor is in a voltage divider with a fixed resistor. The resulting divided voltage is proportional to temperature and the exact temperature can be

determined with the aid of a polynomial or a lookup table. The divided voltage is read by an ADC described in the Data Acquisition System portion of this thesis.

2.6.2 Smart Fuse Circuit

The smart fuse receives power from the DC-DC converter circuit and supplies that power to various loads and monitors those loads for excessive currents. The schematic of a smart fuse is shown in Figure 20.

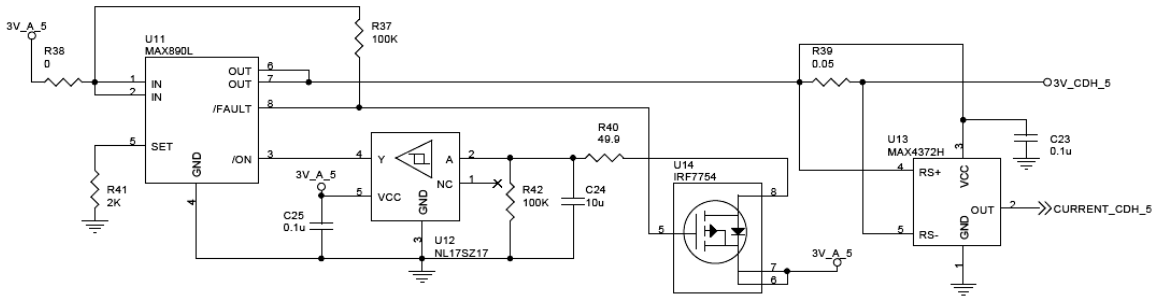

Figure 20. This Smart Fuse circuit acts as a highly programmable fuse.

The Smart Fuse circuit allows the load to receive a programmable maximum amount of current. If the load tries to exceed the maximum current level, the current will limit to 150% of maximum. If the maximum current limit is exceeded for a programmable amount of time, the Smart Fuse will "blow" and shut off power to the load. After power is shut off for a programmable length of time, current is restored to the load and the process repeats itself. Each of these programmable values are set by changing a resistor in the circuit.

The heart of the circuit is the U11, the MAX890L. The MAX890L is a high-side P-channel MOSFET with current limit, a digital ON input and a digital FAULT output. Its current limit is set by a single external resistor. This device has been used on CP1 as a current limited switch under digital control to turn on and off the RF transceivers. The MAX890L in Figure 20 is used to power a load and limit its current, if needed.

When power is first applied to the Smart Fuse, C24 is discharged, the input and output of U12 is low, and /ON is low. With /ON low, U11 turns on and power is supplied to the load. As capacitance on the load's power branch is charged up, the current given to charge the capacitors is limited by the Smart Fuse. During this current limit, the /FAULT output falls low and indicates that the output is exceeding the maximum rated current. /FAULT activates the P-channel MOSFET U14 which charges up C24 through R40. The load must cease current limiting the MAX890L before the shut-off time. Once the load capacitance charges up and the load operates properly, the current supplied to the load decreases below the maximum current. This causes /FAULT to become inactive and C24 ceases to charge. Since the load did not cause an excessive current (and therefore a fault) for a long enough time, U12 never sent a high signal to /ON to shut off the load.

Once the load is on and operating properly, C24 slowly discharges through R42 and the MAX890L continues supplying power to the load.

If a short or a SEL (Single Event Latchup) occur and the current increases above the current limit, the MAX890L limits the current to 150% of maximum. During this over

current condition, the /FAULT output causes U14 to turn on and charge C24. After a preprogrammed amount of time, the voltage on C24 trips the Schmitt trigger buffer in U12 and /ON goes high. A high voltage on /ON turns off the MAX890L and turns off the load. With the load turned off, the /FAULT output of the MAX890L is inactive high and U14 stops charging C24.

C24 then slowly discharges through R42. Once C24 discharges to a low voltage, U12 detects a low voltage on the Schmitt trigger buffer and /ON goes low. The MAX890L is re-enabled and the load is again activated. If the load operates properly and does not consume a current greater than the maximum current for more than the preprogrammed time, the load will stay activated. If the load continues to consume power for longer than the preprogrammed time, the load is shut off until C24 again discharges.

Programming Set Points The characteristics of the Smart Fuse can be changed by modifying any of three resistors. R38 controls the maximum load current set point. The equation to determine the value of R38 given the maximum current set point is shown below:

$$R_{set} = 1380 / I_{limit} (\Omega) \qquad \text{(equ. 7)}$$

The value of I_{limit} is the maximum allowable current through the smart fuse given in amps.

The value of R42 determines the "off time" of the Smart Fuse. A large resistance here will make C24 discharge very slowly and the Smart Fuse will stay off for a long period of time before turning on again. The off time can be determined roughly by the following equation. The equation for the off time is not very accurate between boards and over temperature. For this reason, the following equation should be used only as a guide.

$$Toff = R24 * C24 * 0.6 \text{ (s)} \qquad \text{(equ. 8)}$$

The value of R40 determines the "current limit time" of the Smart Fuse. Increasing the resistance of R40 increases the time that the smart fuse will permit the load to consume current greater than the current limit before shutting off the load. This value should be larger than the time required to bring the load voltage to its final value.

$$T_{climit} = R40 * C24 * 0.55 \text{ (s)} \qquad \text{(equ. 9)}$$

An interesting idiosyncrasy of the Smart Fuse is that the current limit time for the load is greatest when power is first applied to the Smart Fuse. When power is first applied, the voltage on C24 is negligible and the time to charge up and shut off the fuse is greater than the time required if C24 was at the Schmitt trigger's lower threshold. Equation 2 above is valid during normal Smart Fuse operation. The current limit time when the Smart Fuse is first turned on is greater than the time calculated in Equation 2.

Determining the correct resistor values before the circuit boards are manufactured is not feasible since full device functionality will not be complete at that time. Therefore, the three characteristic determining resistors are set to a default value during board manufacture and assembly. Once the boards are populated and the loads are functioning, determining appropriate resistor values and modifying the circuit with correct value resistors will be a simple matter.

The average energy consumed due to a short is an important value for the Smart Fuse circuit. When the load is shorted, the Smart Fuse will periodically supply power to the load whether the short exists or not. The power consumed by the shorted load should be minimized by having a long off time, a short current limit time, and a low current limit. The power consumed due to a shorted load is defined by the following equation:

$$P_{short} = T_{climit} / T_{off} * 1.5 * I_{limit} \quad \text{(Watts)} \qquad \text{(equ. 10)}$$

Smart Fuse Alternatives There are a few alternatives to the Smart Fuse circuit under consideration. One alternative is the standard fuse. They come in fast and slow blow types. There are surface mount fuses with current ratings in the range that we need. The main problem is the lack of resetability we need to prevent permanent failure due to intermittent short circuits and SELs.

Another alternative to the Smart Fuse is a PTC (Positive Thermal Coefficient) fuse. This fuse contains a temperature dependent resistor which increases resistance exponentially

when heated. If an excessive current condition exists, the resistance of the PTC increases dramatically and decreases current flow to very low levels. Once power is turned off, the PTC cools and its resistance reduces to a minimal value. The advantages to this type of fuse are that it is self resettable and requires very little space. One problem with this type of fuse is that it only resets when the load current is reduced to zero. In CP2, the power system is designed such that power to the loads (except for the RF amplifier) is not controlled by a microcontroller. This means that the load current could not be reduced to zero to reset the PTC without adding a power switch and adding a single-point-of-failure to the power system.

Another disadvantage of the PTC fuse is the ambient temperature effect on current carrying capacity. Figure 21 below gives an example of temperature effects on trip current. Curve C demonstrates the significant variation in current carrying capacity on PTC fuses over -20 to +65° C.

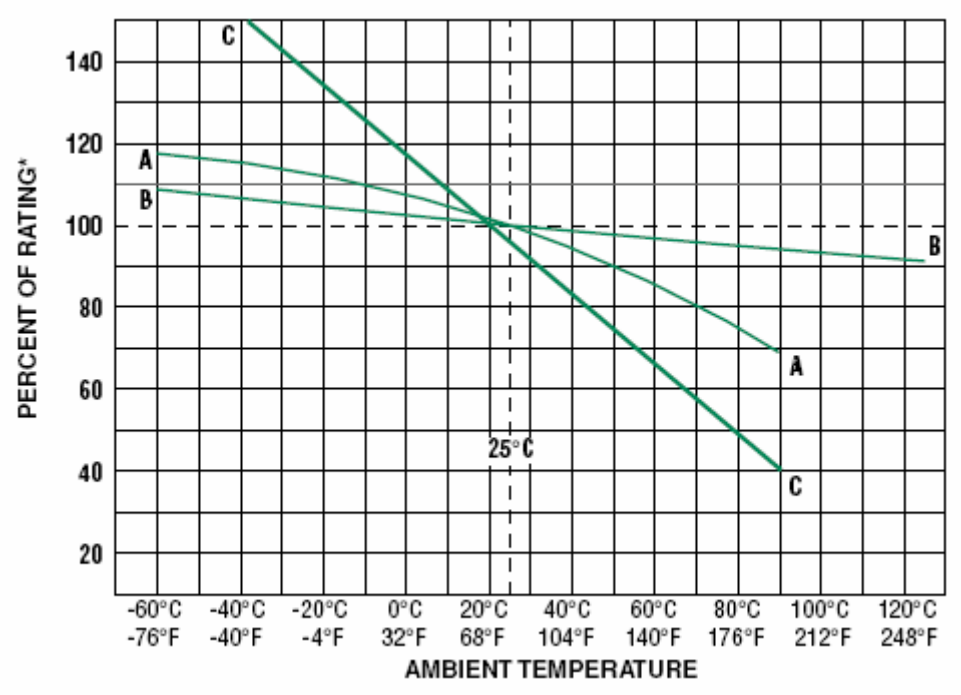

Figure 21. Current carrying capacity of fuses are affected by temperature.[11]

Figure 21 demonstrates current carrying capacity changes in Little Fuse™ fuses. Curve A indicates the effect of temperature on thin film fuses. Curve B demonstrates the effect of temperature on Fast acting and slow blow fuses. Curve C demonstrates the large effect temperature has on PTC fuses.

Our Smart Fuse design will vary in current limit by ±10% plus the slight variation in resistor resistance over -20 to +65° C.

3 Command and Data Handling and Data Acquisition

The CP2 bus must have a system that coordinates data flow and processes information. This system is called the Command and Data Handling (C&DH) system. The Data Acquisition (DAQ) system is an integral part of the CP2 bus and works closely with the C&DH system to provide critical health and status information. The C&DH must be able to communicate with the payload as well as with the RF communications system, process and store data, monitor its own health, and even autonomously respond to changing circumstances and environments. Both the C&DH and the DAQ must be robust and resistant to failures. For example, failure on a non-critical portion of the DAQ should not prevent critical information from passing through CP2's data bus.

The main tasks of the C&DH are as follows:

- Interpret and execute received commands from the Communications system
- Packetize data for Communications system transmission
- Institute peak power tracking on each solar panel
- Retrieve health status information from various temperature, voltage, and current sensors on CP2
- Process and respond to health status information
- Store and buffer sensor data, error codes, and other important information
- Provide a storage location for payload data before the data is uploaded to earth
- Activate the payload and possibly process payload data

- Minimize loss in the event of a bus failure

The main task of the DAQ is to provide the C&DH with the means to:

- Acquire health status information
- Acquire attitude determination information

Features which the C&DH and DAQ systems should both have are:

- Low part count for small circuit sizes
- Low power consumption
- Failure isolation
- A simple data communications bus

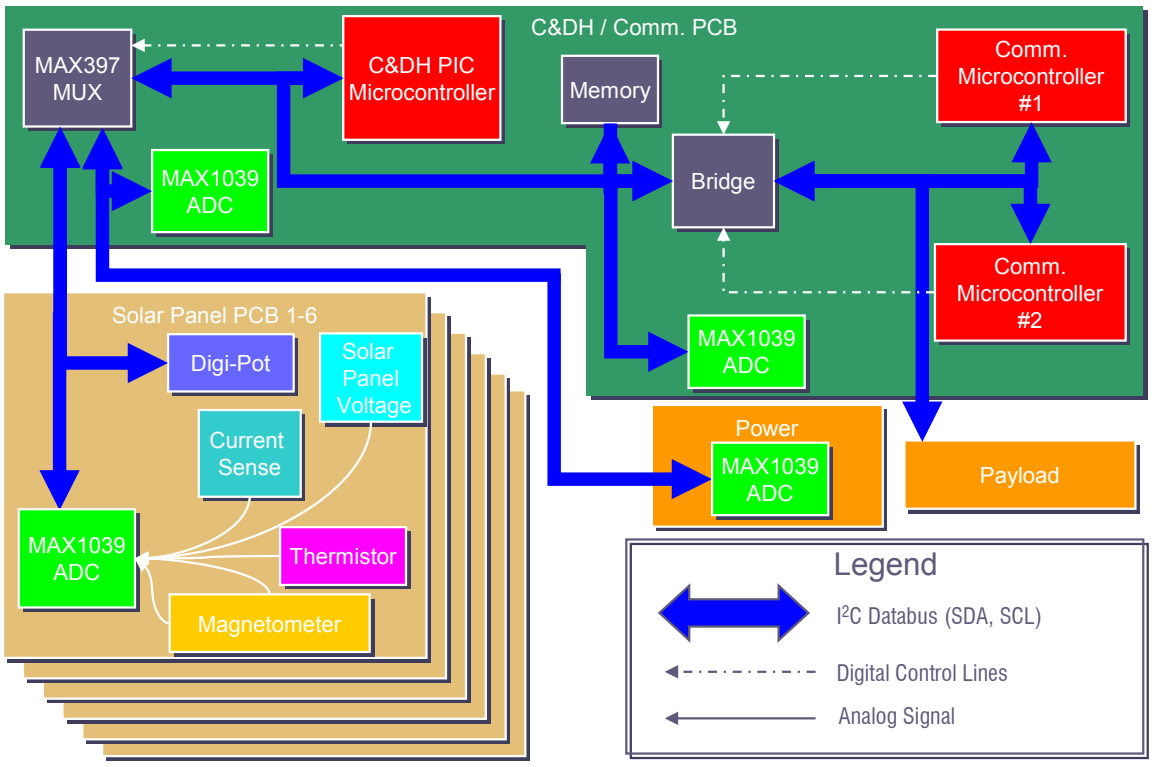

Figure 22. C&DH and DAQ block diagram.

Figure 22 illustrates the C&DH and DAQ used on CP2. The C&DH system includes the command and data handling processor that performs most high-level functions on the CP2 bus. The I^2C two-wire bus allows the C&DH processor to communicate with other devices. The C&DH processor uses two FLASH memory devices for medium and long term data storage. The Comm. microcontrollers communicate with the C&DH processor for processing of received commands or to have data downlinked to earth. The payload receives commands and transfers payload data to the C&DH system. The C&DH processor also retrieves data from sensors located on the CP2 bus through the DAQ.

The system is designed with capability and failure isolation as two key elements. The entire system has nearly 100 data points from various sensors across the satellite. To collect all of this information, a multiplexer is used to select between 8 different I^2C branches. Six of the branches connect to side panels. Every side panel collects solar power information, temperature, and attitude control information. When the C&DH processor collects side panel data, it selects a particular side panel by setting the MUX channel and communicating to the side panels' I^2C branch. The next MUX channel is then selected for communication with the next side panel, and so on. There are also sensors on the C&DH and Power boards. These sensors are each selected with separate MUX channels as well.

The advantage of this system is two-fold. First, isolating I^2C branches allows redundant devices addresses to be used. It is convenient to create side panels as identical as

possible. One side effect of this is that the I^2C devices on each side will have identical I^2C addresses and cannot be on the same I^2C bus. By isolating the I^2C branches through a MUX, no two branches are active at the same time and the problems caused by multiple devices with the same address on the same bus is prevented.

Second, any failure on an I^2C branch is isolated in that branch. The failure only affects the entire bus system when the failing branch is selected. When the C&DH processor detects a failure on an I^2C branch, the branch is determined to be faulty and is skipped in further branch selections.

To further isolate I^2C bus failures, the main I^2C bus, which contains the C&DH processor and external memory, can be isolated from a small, "Contingency," bus which connects only the most basic systems required for CP2 to successfully complete its mission. The contingency mode is enabled when either Communications controller detects a failure on the main I^2C bus. When this occurs, the bridge that connects the main bus to the contingency bus is opened. This leaves only the Communications controllers and the payload on the Contingency bus. In Contingency mode, the Communications controllers can activate the payload, collect data from it, and transmit the unprocessed data back to earth in an effort to complete CP2's mission even if there is a failure on the main I^2C bus or the C&DH processor has failed.

As designed, the C&DH system and the Data Acquisition system on CP2 are not as robust and-fault tolerant as their counterparts in larger satellites, but they are capable of

operating with several types of system failures within a volume, mass, and power constraint which their large satellite counterparts cannot match.

The primary side of the C&DH board is shown in Figure 23. The primary side contains the C&DH board data acquisition system and both communications processors. The secondary side of the C&DH board is shown in Figure 24. The secondary side contains the C&DH processor, FLASH memory, both RF transceivers, and both RF amplifiers. These images are of a test board that is not in flight configuration.

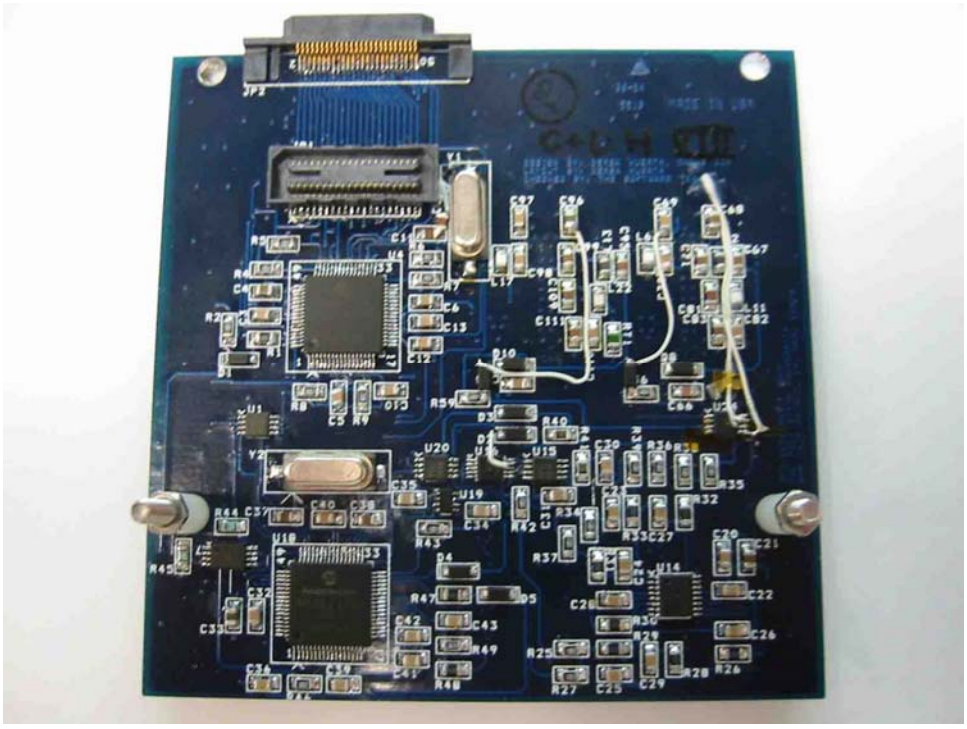

Figure 23. Primary Side of C&DH Board.

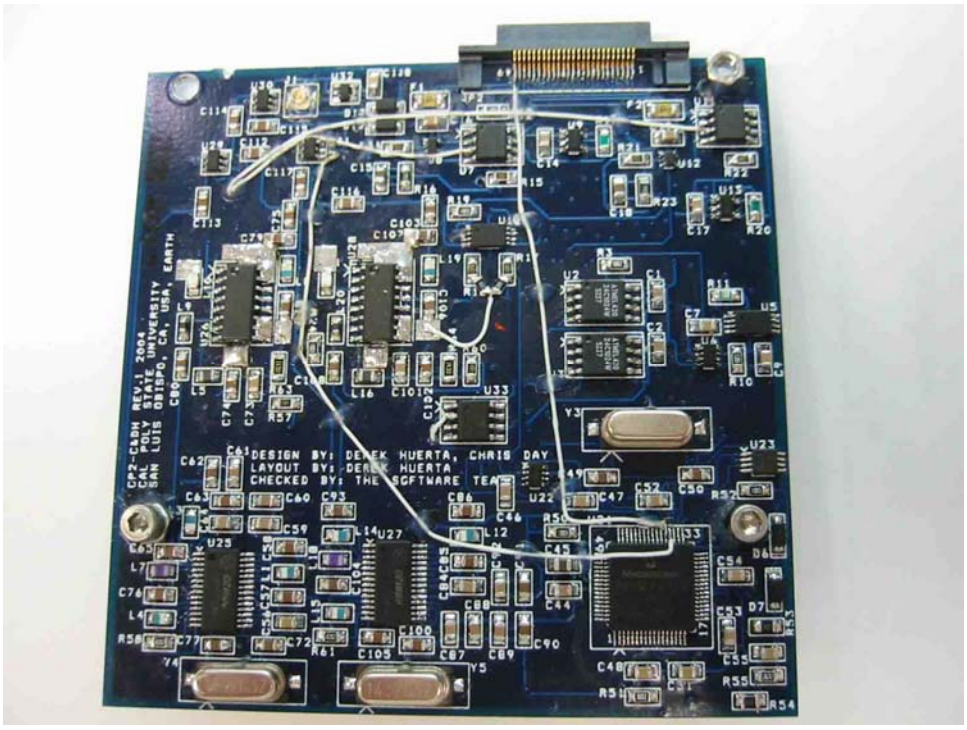

Figure 24. Secondary Side of C&DH Board.

3.1 Choosing the I^2C Bus

A bus is needed to allow data flow inside the C&DH system as well as to the Comm. system and the payload. There are several types of buses that can accomplish this. The two basic types of buses are parallel and serial. Parallel buses have very high data rates and are needed for most high-volume, low physical distance data transfers. Serial buses have relatively lower data rates because every word of data must travel through the bus bit by bit instead of all together. Serial buses are commonly used whenever low wire counts are preferable such as long distance communication or space constrained electronics equipment.

As we are space constrained and do not need an extremely high data transfer rate, we choose to use a serial bus instead of a parallel bus. This decision allows devices using the bus to have a lower pin count and thus consume less space. The layout of the Printed Circuit Board (PCB) is also simpler as there are fewer wires to route. This also allows us to take advantage of specialized sensors which communicate using a serial bus protocol.

The next task is to determine the most useful serial bus protocol. We determined that the following are the most useful attributes for CP2's serial bus protocol:

- One or two pins required
- Data rates higher than 9600 baud
- Availability of temperature sensors, ADCs, and other devices
- Low power
- Availability of digital potentiometer for peak power tracking
- Simple software implementation

The bus protocols that we considered are:

- 1-wire bus™ .
- SPI – Serial Peripheral Interface bus.
- RS-232, RS422, and RS-485, +-12V and +5V based buses.
- I^2C – Inter-Integrated Circuit.

3.1.1 1-wire bus™

The 1-wire bus™ is a single wire serial bus created by Dallas Semiconductor. It is used to communicate between many Dallas and Maxim devices such as temperature sensors, EEPROMs, I^2C bridges, UARTS, and other devices. Its advantages are that it can interconnect several devices using a single wire. Also, a wide variety of 1-wire devices can be powered from the same wire that also carries data.

One disadvantage of this bus is that the addressing scheme to select one of multiple devices on the bus is rather complex. To mitigate this, Maxim has written source code in C, VB, and other languages to help 1-wire bus users use the 1-wire bus™.[4] Another disadvantage is that there is very little microcontroller hardware support for the 1-wire bus. To use the bus, the microcontroller must "bit bang" the protocol by running a special subroutine and dedicate itself to transmitting or receiving data via the bus. Many microcontrollers are designed with hardware interfaces for protocols such as I^2C, SPI, and RS-232/RS-485. These hardware interfaces simplify the software required to utilize the bus and relieve the microcontroller of the burden of bit banging.

For CP2, the 1-wire bus would be useful for acquiring data from many different sensors. The disadvantage is that the C&DH microcontroller would have to manually bit bang an I/O pin.

3.1.2 SPI

The SPI bus is a prevalent bus used for communications between microcontrollers and devices such as external EEPROM, UARTS, and other devices. It boasts a fast data rate, reaching up to 10Mbps.[5] The SPI bus uses 3 wires for clock and data plus one additional line to enable each device that the microcontroller can communicate with.

While the SPI bus has an impressive throughput, and many microcontrollers contain hardware support for it, the microcontroller pin count becomes excessive when the number of devices that CP2's C&DH system must use are considered. Also, the SPI protocol doesn't allow for multiple master devices on the bus. This is a feature that we wish to implement on CP2 so that the Comm. Controllers can control the data bus.

3.1.3 RS-232, RS-422, and RS-485

These three serial buses have been around for many years. The RS-232 standard has been in existence for over 40 years now and its use has been on the decline during the past several years. Almost all microcontrollers have support for RS-232 interfaces in the form of a Universal Asynchronous Receiver Transmitter (UART). The RS-232 standard calls for more than two wires but many microcontroller interfaces operate properly by implementing only parts of the protocol.[6]

While the RS-232 protocol specifies data rates to 20kbps, speeds of 115.2kbps or higher are used successfully over short distances. RS-232 is also full duplex which is useful when there is a high rate of bi-directional data flow. However, RS-232 is point-to-point

meaning that it only connects two devices. One possible way to overcome this two-device limit is by using a multiplexer controlled by a master device that selects which slave device to talk to.

The RS-232 protocol specifically calls out a voltage greater than 3V as a logic zero and a voltage less than -3V as a logic one. These voltage thresholds generally require a logic translator to convert the microcontroller logic levels to the levels acceptable for RS-232 communications. When a microcontroller is communicating to another microcontroller, another option is sometimes used. With short distances, usually less than 10 feet, the UARTs of the microcontrollers can be attached together. The transmit line of each is attached to the receive line of the other. With this arrangement the microcontrollers can communicate to each other asynchronously, in full-duplex, with only two wires and no additional hardware.

While using the RS-232 protocol, or parts thereof, is very convenient for certain communications, it does not suit the needs of CP2's C&DH system where multiple microcontrollers and peripheral devices need to communicate with each other. It may, however, be useful as part of the umbilical interface to allow CP2 to communicate with the outside world without the use of the Communications system.

RS-422 and RS-485 are newer protocols which address several shortcomings of the RS-232 serial communications protocol. They both use balanced circuits and thus have

better noise immunity. They both operate at up to 10Mbps or over distances as far as 1200m as defined by their protocol.[7]

RS-422 is a protocol for a single transmitter to communicate, one way, to several receivers. Thus, it isn't very useful for CP2's C&DH system where several devices must communicate bi-directionally. The RS-485 protocol allows multiple devices to communicate to each other in either half-duplex or full-duplex modes depending on the selection of two-wire or four-wire configurations.[8]

The RS-485 protocol requires hardware external to the microcontroller for logic level conversion and balanced line driving. There are also very few, if any, single-chip devices such as temperature sensors and ADCs that use the RS-485 standard.

3.1.4 I^2C

The I^2C bus protocol was created by Philips nearly 20 years ago and has grown to become a popular interconnection bus in embedded applications with over 1000 devices now using the bus. It uses two wires, one as a clock, the other for bi-directional data. The I^2C bus initially specified a 100kHz clock frequency, but further enhancements to the protocol include bus speeds of 400kHz and even up to 3.4MHz. The bus is half-duplex with a common data line which all devices communicate over.

One disadvantage of the I^2C bus is the limited number of device addresses. Each device on the bus has its own built-in address. Some I^2C devices allow pin-configurable

addresses by tying certain pins high or low. If several devices of the same type are placed on the same I^2C bus, even the pin-configurable address may limit the number of like devices on the bus below the desired number. One way to overcome this limitation is to utilize a dual multiplexer (MUX). The multiplexer can select one of several branches and one MUX will multiplex the clock line, the other will multiplex the data line.

Many microcontrollers have I^2C interfacing hardware built in. This greatly simplifies the I^2C software implementation. There are also many discrete devices such as temperature sensors, ADCs, and digi-pots that have a very low pin count and small size, thanks to the limited number of pins required for I^2C communication.

The I^2C bus has a faster data transfer rate and is easier to implement in software than the 1-wire bus. It does not require dedicated enable lines for every peripheral device like the SPI bus has. It allows bi-directional communication between several devices but does not require any external devices except two passive resistors.

Based on the analysis, the I^2C bus is the most suited to our requirements and is the bus chosen for our C&DH system.

3.2 I^2C Multiplexing/Failure Isolation

CP2's C&DH circuit requires the collection data from up to eight different circuit boards. To allow the I^2C bus to connect to each circuit board, a multiplexing scheme is used. A diagram of the multiplexing scheme is shown in Figure 25.

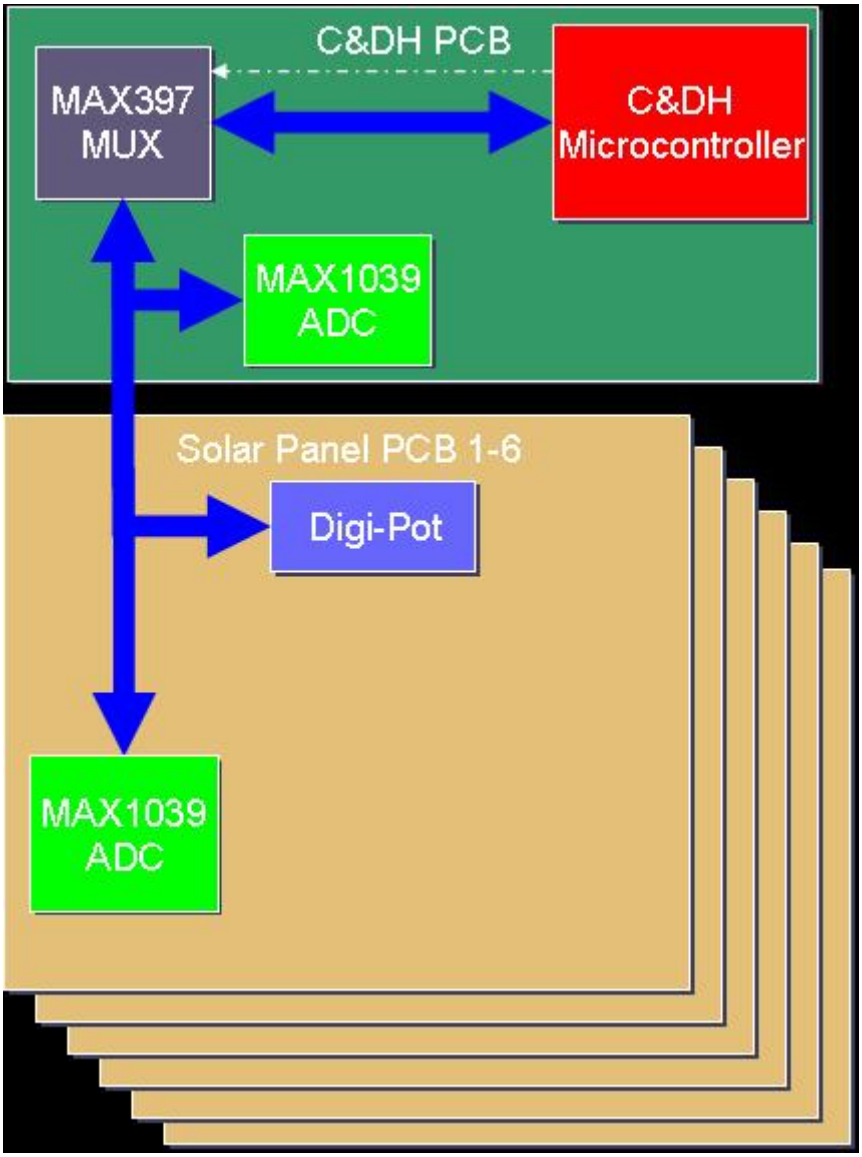

Figure 25. I^2C multiplexing scheme.

One advantage of multiplexing the I^2C bus into branches is to prevent I^2C address limitations because each side panel will be identical to the next. With each side identical, the manufacturing costs and design time will be reduced but at the expense of I^2C address flexibility. Each side will have to have I^2C devices with identical addresses unless a creative use of cutable traces is employed. The multiplexing allows each side to be individually selected and all other sides to be deselected.

Not only does this scheme allow several devices with the same address onto the I^2C bus, it can also isolate an I^2C branch that has a failed device. A failed device on the I^2C bus can hold one or both of the bus lines low and prevent any further data transfer, thus preventing the flow of information on CP2 and crippling the satellite.

If an I^2C bus failure does occur on a branch, the C&DH processor can notice the I^2C bus failure and select a different branch. That branch can be marked as bad by the C&DH processor which can then no longer use the branch or try the branch again after a predefined interval.

For the multiplexing, we used the MAX397. This device contains two analog 8:1 multiplexers and allows multiplexing of both I^2C bus lines with a single IC. The multiplexer selects between eight different branches: one branch for each side panel and one branch for each of the two inner bus boards.

3.3 Data Acquisition Circuits

Data acquisition circuits are embedded in every PCB on the CP2 bus. They are each very similar to each other. In fact, all side panels and the front panel have identical data acquisition circuits. The data acquisition circuits on the C&DH/Comm. board and the Power board differ from the other data acquisition circuit only by what they sense.

3.3.1 Side Panel and Front Panel Data Acquisition

Every side panel's data acquisition circuit measures several data points. This circuit measures temperatures, voltages, and currents at various points on the panel. The basic parts of the side panel data acquisition circuit are shown in Figure 26.

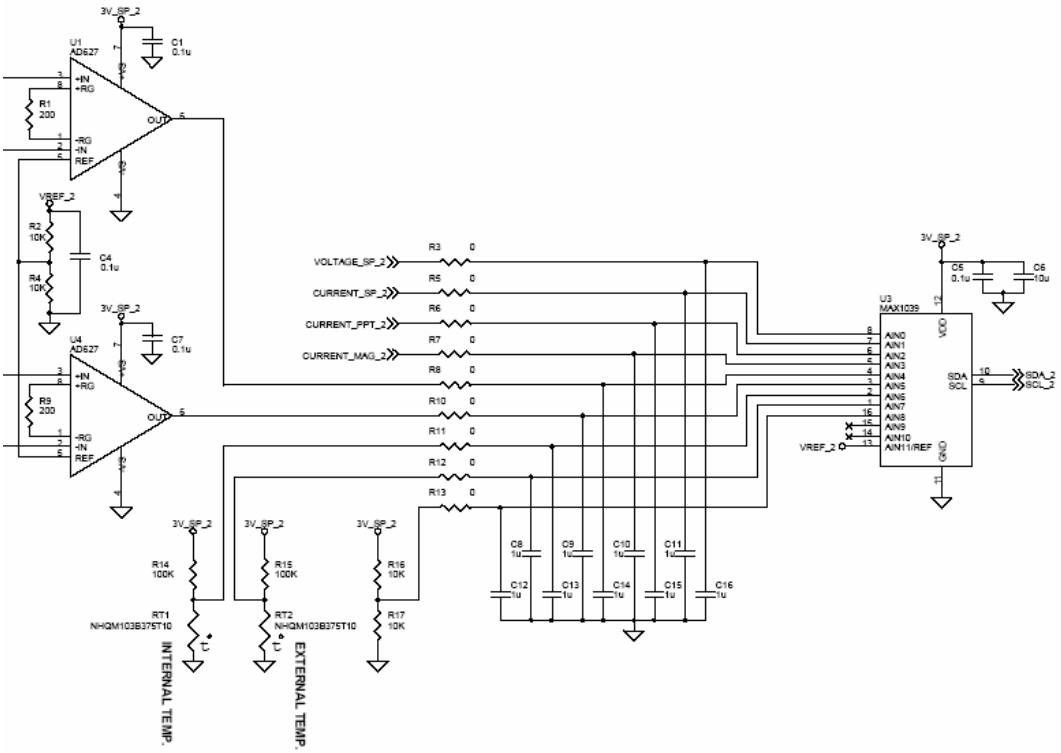

Figure 26. The data acquisition circuit for side panels.

The heart of the data acquisition circuit is the MAX1039 analog to digital converter (ADC). This device can read 12 analog inputs with 8 bits of resolution at up to 188k samples per second. This device was chosen because we needed a simple, single chip ADC solution that will connect directly to the I^2C bus. While there are other ADCs that interface with the I^2C bus and convert analog data with higher resolution, higher resolution data is not needed and would increase data storage requirements and I^2C bus transaction times. The MAX1039 also contains an internal voltage reference which removes the need for an additional component and the reference voltage can be also supplied to any external circuitry requiring it.

There are four types of sensory data acquired by the ADC: temperature, voltage, current, and magnetic field strength.

Temperature Measurement The temperature is measured by the NHQM103B375T10 thermistor designed by Thermometrics. These thermistors are much like the thermistors successfully designed and tested on CP1. The thermistor will change resistance with temperature and the temperature is converted to a voltage by using the thermistor in a voltage divider. In Figure 26, RT1 and RT2 are the thermistors and R14 and R15 are used with the thermistors to create an analog voltage that will then be sensed by the ADC.

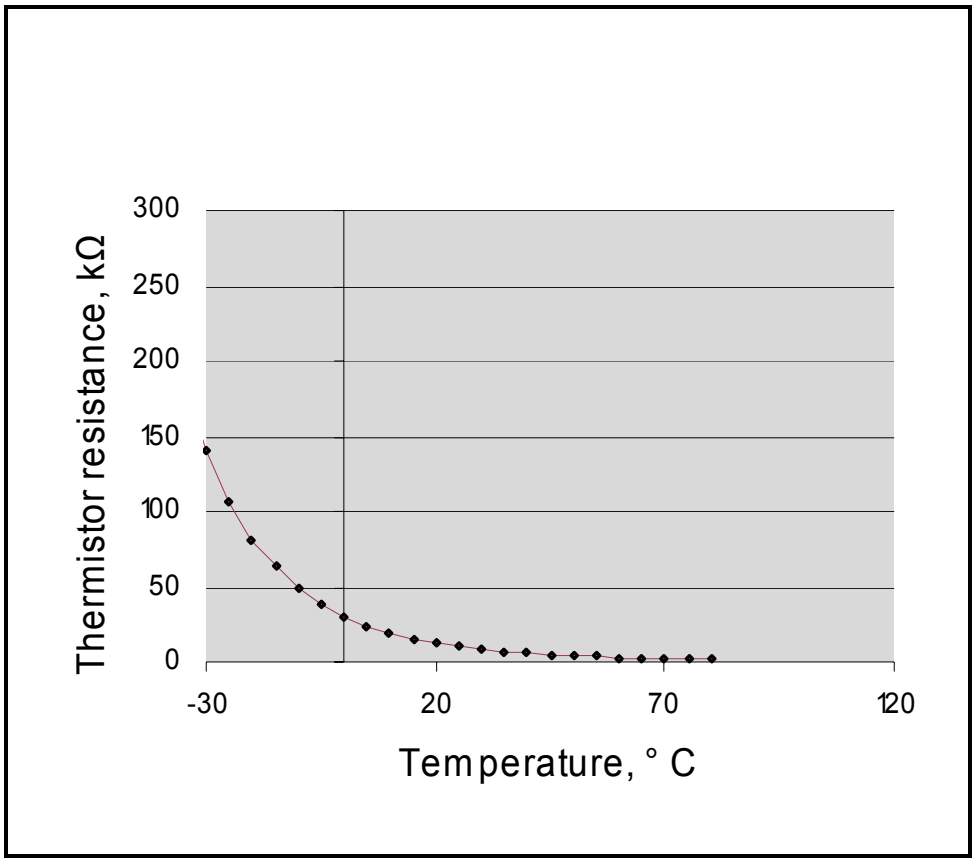

Figure 27. Resistance to Temperature Relationship for a NHQM Series Thermistor by Thermometrics. [9]

The thermistor resistance is a log function of the temperature. This makes the voltage out of the voltage divider highly non-linear. The resistance to temperature curve is shown in Figure 27. The ADC has an analog input voltage range from zero to two volts. With the ADC input voltage range and resolution known, a graph ADC code to temperature has been created. This graph is shown in Figure 28.

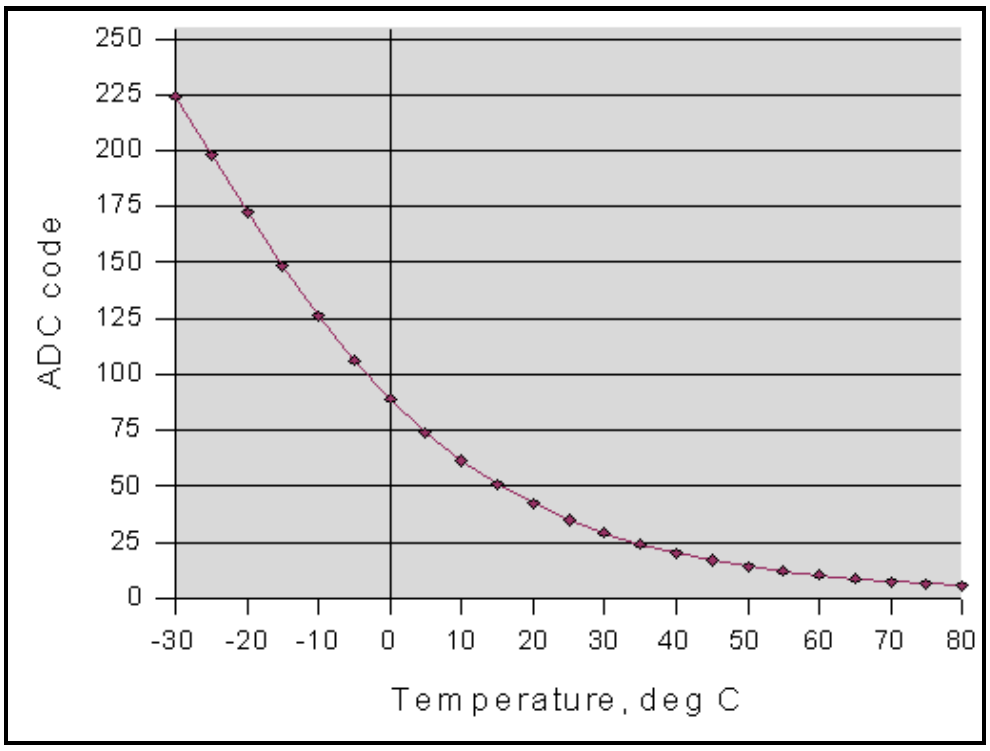

Figure 28. ADC Code vs. Thermistor Temperature.

The values of the 10kΩ thermistor and the 100kΩ resistor in series with it have both been chosen for a few reasons. First, the 100kΩ resistor has been chosen because it prevents the maximum current consumption through the temperature sensing circuit to be a maximum of 30uA. The actual current consumption varies with the thermistor's resistance. Resistances considerably higher than 100kΩ cause the input leakage current of the ADC to affect the accuracy of the temperature measurement.

The 10kΩ thermistor's value is selected because it gives an appropriate range of temperature over which the ADC will receive an appropriate voltage range. The thermistor voltage divider circuit is supplied with 3V from the regulated side panel 3V line. Since the thermistor will vary the voltage divider's output voltage and the ADC has

an input voltage range of 0-2V, the thermistor resistance must not cause the ADC's input voltage to reach above 2V over the operating temperature range of the satellite. In order to keep the resistor divider voltage in the correct range, the 10kΩ thermistor is selected. This thermistor resistance value give a voltage in the range that the ADC can read between temperatures of -35°C and 80°C. The 10kΩ thermistor's resistance value means that its resistance is around 10kΩ at 25°C.

From Figure 28, it is clear that the ADC codes change less frequently at higher temperatures than at low temperatures. It is desirable for ADC codes to change frequently as it gives better resolution. For example, if the temperature changed by 0.5°C per ADC code, this would provide a one half degree temperature sensing resolution. While the temperature sensing resolution is very good or adequate over most of the operating temperature range, the number of degrees per ADC code increases significantly near the upper end of the operating temperature range. For example, at 60°C, the temperature sensing resolution is 3°C per ADC code. While this is a widely spaced temperature resolution, we do not need a very precise resolution and this circuit meets our requirements.

The Thevenin equivalent resistance of the thermistor voltage divider as seen from the ADC varies widely and can affect the accuracy of the ADC reading. The ADC's input leakage current can reach +-1uA and the resistance of the voltage divider is between 58kΩ and 1.4kΩ. This range gives a worst case error of about 7 ADC codes at -30degC and 4 ADC codes or less at -10degC and higher temperatures.

Some other methods of converting temperature to an analog voltage are with a temperature sensing IC such as the LM20 series or with a thermocouple and thermocouple interface using an IC such as the AD594.

Voltage Measurement Two different voltages are monitored on the side panel. They are the regulated 3V supply and the solar panel voltage.

The voltage on the 3V supply is too great to be monitored by the ADC directly. Instead, the 3V line is divided in half. By doing so, the voltage range that the ADC can now monitor is 0 to 4V. The resistance of the resistors are high enough that the power consumed by the voltage divider is less than 1.5mW. The resistance is also low enough that the input leakage current of the ADC causes a 5mV or lower error. This error represents less than the resolution of one code.

The solar panel voltage can be as high as 5.2V if the solar panels cool to –30degC. To measure the solar panel voltage with the ADC's 0 to 2V input voltage range, the solar panel voltage is divided by three using a 10 kΩ resistor and a 20kΩ resistor. This resistor voltage divider consumes less than 1mW with a solar panel voltage of 5.2V.

Current Measurement The current into and out of the peak power tracker, as well as the current consumed by the magnetometer, is measured using current sense amplifiers. The current is first sent through a low impedance resistor called a current sense resistor.

For all three cases, the resistance is 0.05 Ω. The voltage drop across the resistor is then sensed by a high-side current sense amplifier, the MAX4372H. This device outputs a single-ended voltage 100 times greater than the differential voltage across the current sense resistor. This output voltage is then sent to the ADC. The power lost to the 0.05 Ω resistor is only 8mW with a current flow of 400mA. 400mA is the largest current seen by the current-sensing circuits.

Magnetometer Measurement To assist in attitude control, or orientation control, magnetic field measurements are collected on CP2 using devices called magnetometers. These magnetometers use material which changes resistance with magnetic field. The magnetometer used on CP2 is a Honeywell HMC1052. This magnetometer contains a two-axis magnetometer with each axis sensor in its own H-bridge configuration. The output of the magnetometer is a differential voltage which needs amplification. To amplify the signal, an AD627 instrumentation amplifier is used. The differential output of the amplifier has a peak to peak value of around 1.0 gauss in a 700km orbit around earth. With this span of magnetic field, the variation of the magnetometer output voltages is about 1.5mV. This differential voltage is amplified by the instrumentation amplifiers by 1000 times and an offset is given to the output voltage so that negative magnetic field measurements can be read as positive voltage values. The resulting voltage is centered around 1V and has a span of around 1.5V. This span and offset give a voltage from 0.5 to 1.5V, well within the input voltage range of the ADC.

Low Pass Filter Before analog signals are read by the ADC, they are sent to a first order low pass filter before being read from the ADC. This filter screens out electrical noise coupled into the analog signal from adjacent circuits or from the RF communications system. The filter is implemented with a single resistor and capacitor for each analog input. The resistance and capacitance needed can be determined using circuit analysis in the frequency domain given an appropriate break point of the low pass filter.

Another method to determine values is to determine the appropriate time constant, tau, for the low pass filter. τ should be at least one fifth as long as the sampling rate of the signal being measured. With τ at one fifth of the sample rate, the worst case error is less than 1%. Using the equation $\tau = R*C$, the values of R and C can be quickly determined.

When determining the values of resistance and capacitance, the resistance is kept low enough that the input leakage current on the ADC (±1uA in this case) is negligible. To keep the error less than ½ LSB, the maximum series resistance can be found using Equation 1. For this case, the maximum resistance to give an error better than ½ LSB is 4kΩ.

$$R_{\max} = \frac{2.048V}{256 * 2 * 1uA} \quad (\Omega) \qquad \text{(Equ. 11)}$$

The low pass filter values have not been determined during the design process. This is because the EMI noise that the low pass filter screens out cannot be determined accurately before the circuits are activated on circuit boards mounted in the satellite.

3.3.2 C&DH/Comm. Board Data Acquisition

The C&DH/Comm. Data Acquisition circuit is simpler than the side panel data acquisition system. The C&DH/Comm. Data Acquisition circuit is shown in Figure 29.

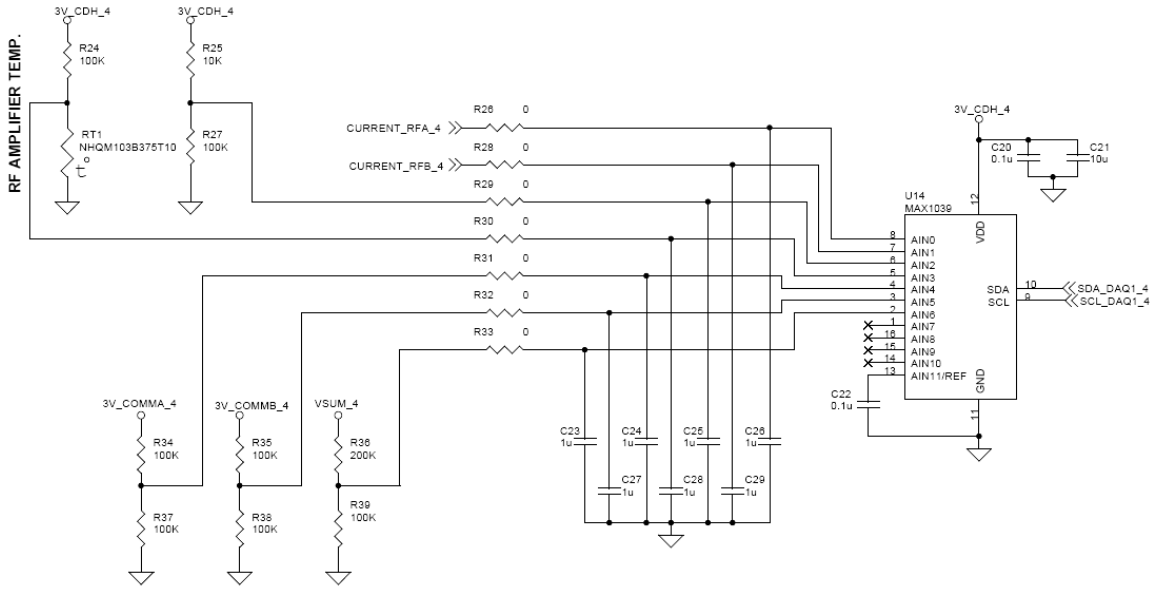

Figure 29. C&DH/Comm. Data Acquisition circuit.

The C&DH/Comm. board needs careful monitoring of its RF amplifiers. The amplifiers consume a considerable amount of power and are the greatest heat producers on the CP2 bus. Therefore, the data acquisition circuit monitors both the current consumed by the RF amplifiers and the temperature of the RF amplifiers.

The C&DH/Comm. Data Acquisition circuit also monitors four voltages used on the board: the 3V Comm. A, 3V Comm. B, 3V C&DH, and the battery voltage used by the RF amplifier.

The current is sensed in much the same way as the current sensors on the side panels, the only difference is the type of MAX4372 used. The maximum current measured here can reach 1.2A whereas the maximum current measured on the side panels is 400mA. To modify the current sensing circuit, we simply choose a MAX4372 which amplifies the current sense resistor voltage less than the MAX4372H does. The MAX4372T multiplies the current sense voltage by 20. With this amplification factor and a current sense resistance of 0.05Ω as before, the maximum current that can be sensed comes out to be 2A. With this maximum current, the resolution of the current value being read by the ADC is 7.8mA.

The energy consumed by the 0.05Ω resistor is greater than the current consumed on the side panel because of the greater currents. With the maximum current of 1.2A, the power consumed by the current sense resistor is 72mW. This value is much higher than the power consumed on the side panels but, because the amplifier consumes around 3.5W of power, the current sense resistor only consumes about 2% of the power consumed by the RF amplifier.

The voltages measured on the C&DH/Comm. Board are measured in a fashion identical to the side panel's voltage measurement circuits. The low pass filter circuit is also identical in that each analog signal is individually filtered with a RC low pass filter. The resistor and capacitor values for these filters will also be modified while testing and debugging.

3.3.3 Power Board Data Acquisition

The Power Board Data Acquisition circuit is designed to monitor several of the voltages, currents, and temperatures of the power system. The currents measured are the C&DH, SPA, SPB, Comm. A, Comm. B, and payload current. The voltages measured are the SPA and SPB voltages. The other voltages are measures on other boards closer to the point of load. The temperatures of each of the three DC-DC converters are also monitored. Figure 30 describes the Power Board Data Acquisition circuit. Battery data is collected separately and is described at the end of this section.

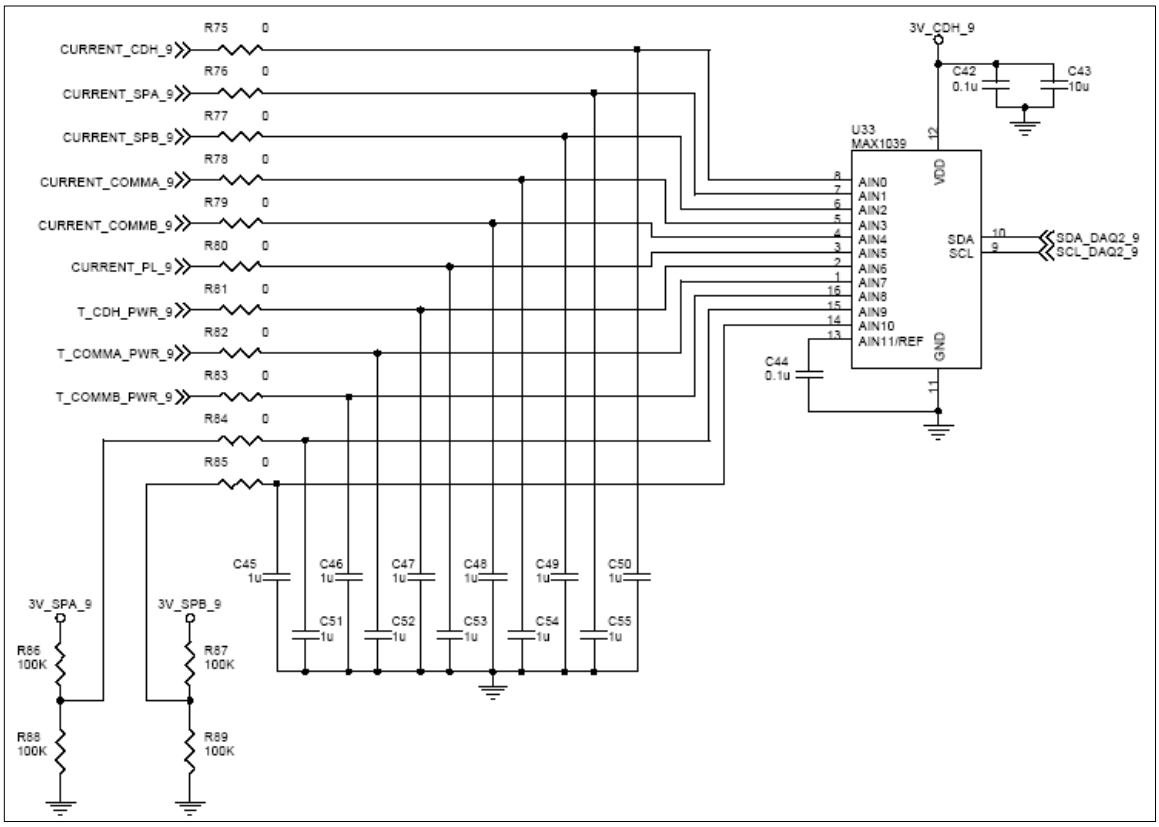

Figure 30. Power Board Data Acquisition Circuit.

The currents are each measured in a fashion identical to the side panel current sensors except for the payload current sensor. The payload current may reach up to 1.2A. The payload current sensor is designed identically to the RF amplifier current sensor used on the C&DH/Comm. Board.

The Power Board measures two voltages, SPA and SPB. These two voltages supply regulated 3V to the side panels on the CP2 bus. The side panels with odd numbers are powered by SPA while the side panels with even numbers are powered by SPB. With this divided approach, we don't need the board real estate required for individual power supplies for each side panel and we don't lose power to all side panels if a fault occurs on one side panel. The voltages of SPA and SPB are measured on the Power Board with the same voltage sensing circuit used on the side panels. The voltages are divided down in such a way that the regulated voltage is well within the zero to two volt voltage range of the ADC.

The temperatures of the DC-DC converters are also monitored. If the voltages lose regulation or a failure of a DC-DC converter occurs, this temperature information will aid in determining if the DC-DC converter temperature was part of the cause. The temperature is determined using a thermistor in the same circuit used to measure temperature on the side panels.

In addition to the Power Board sensors described above, the two DS2761 battery monitors on the Power Board collect additional information on battery conditions. Each of the two batteries has the following characteristics monitored:

- Battery current measured to 0.625mA
- Battery accumulated current to 0.25mAh
- Voltage measurement to 4.88mV
- Temperature measurement to 0.125deg C
- Current and past battery protection status

All of these measurement functions are performed internal to the DS2761 IC. The information is sent to the C&DH processor through a one-wire bus that allows bidirectional communication between the C&DH processor and the DS2761.

3.3.4 I^2C Power Branch Isolation

A possible problem occurs when different devices on the I^2C bus are supplied power by more than one power branch. If power is lost to one branch, but not another, then two problems could occur.

One problem is that the powered down branch could pull the I^2C lines low through the almost ubiquitous ESD protection diodes found in modern ICs. Pulling the I^2C lines low would completely disable the bus and prevent any data transfer. The other problem is that the powered down branch may also be able to power itself from the I^2C bus lines.

The same ESD protection diodes which could keep the I^2C lines low also have the potential to allow the voltage on the I^2C bus to power the "powered down" IC as well as the other devices on the same power branch. Even through the I^2C bus lines probably will not be able to bring the power branch to the normal operating voltage, bringing the power branch to a fraction of the regular supply voltage may cause some ICs to begin operating, possibly incorrectly, when they should be powered down. The partial or full operation of devices or entire circuits on a power branch that should not have power may jeopardize the operation of correctly operating circuits by giving false signals.

To solve this problem, I^2C isolation circuits such as the one in Figure 31 are implemented whenever the I^2C bus is used by devices on a power branch.

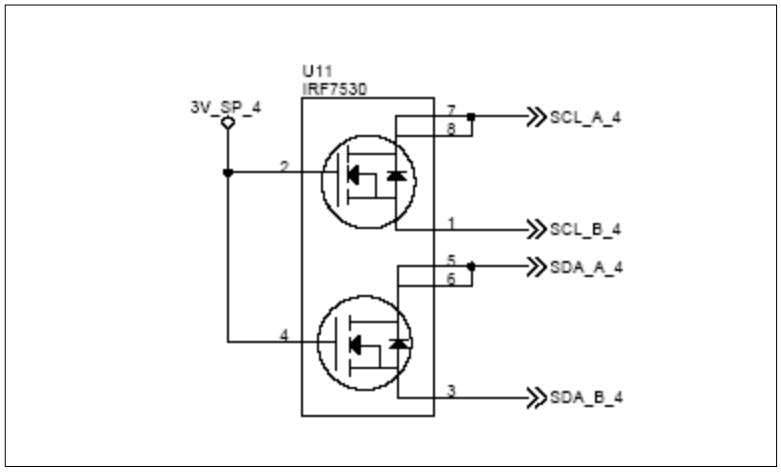

Figure 31. I^2C Isolation Circuit.

This circuit performs isolation by disconnecting I^2C devices on each power branch from I^2C devices on the other power branches. The operation is much like a gate that allows

bi-directional current flow while the gate is open but prevents current flow from entering when the gate is closed. When power is removed from a power branch, the MOSFETs turn off. The parasitic body diode can still be active, though. To prevent the body diode from allowing current to flow from powered power branches to non-powered branches, the MOSFETs are oriented in such a way that the powered branches are attached to the Cathode of the diodes. Thus, the powered branches will never be able to supply current through the diode and allow the I^2C signal into the powered down branch.

This isolation circuit is very similar to the I^2C level shifter described by Philips and shown in Figure 32.

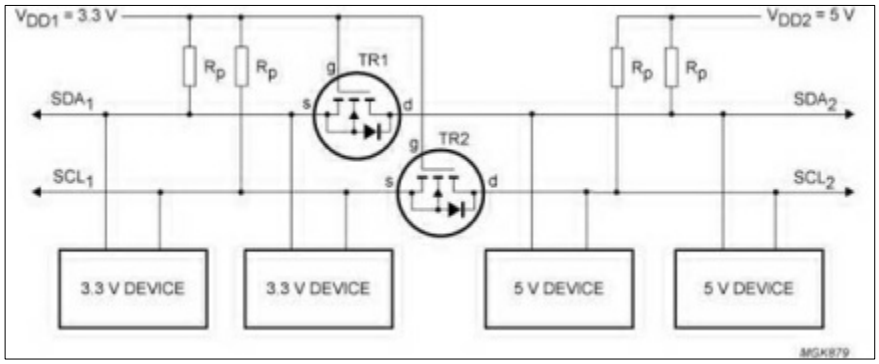

Figure 32. I^2C level shifter designed by Philips Semiconductor.[10]

3.3.5 Choosing the C&DH Processor

The search for a suitable C&DH processor began by identifying useful attributes for the processor. The following list summarizes the pertinent attributes sought after for our C&DH processor:

- Low power (<5mA) at throughputs at and below 1MIPS.
- Low voltage (3V) operation.
- On board RAM of at least 1kB.
- On board ROM of at least 64KB.
- Built in I^2C bus hardware interface.
- Several general purpose I/O pins (GPIO).
- In circuit programmability.

The search for the best processor was lead by Pat Hall and the choice came down to two families of processors.

One family of microcontrollers is created by Silicon Laboratories, formerly Cygnal inc., and runs an 8051 core. Theses processors are designed to be used in low power, automotive, appliance, and mechatronics applications. For our requirements, the high end models meet all of the above criteria including a 4mA power consumption when operating at an average of 2MIPS, 128kB Flash memory, and 8448B of internal data RAM. These processors include a single cycle 8 by 8 multiplier engine for faster data processing.

The other family is the PIC18 family of PIC microcontrollers by Microchip. These processors are designed for embedded systems and are frequently used by hobbyists because the processors are cheap or available as free samples and the development software and hardware is also inexpensive. Various PIC processors have also flown in

space on AMSAT satellites. A “C” compiler is available for PICs and operates inside of the standard PIC integrated development environment. The PIC18LF6720 is the processor singled out as the best choice in the PIC family. This processor consumes around 2.5mA at 3V while running at 4MHz. With that clock rate, it processes at up to 1MIPS. It contains 128kB of FLASH memory and just under 4kB of RAM. It has internal I^2C interface hardware and 52 I/O pins. The processor can also be programmed from three pins while it is still imbedded in the application circuit. With this in circuit programmability, CP2’s processors can be reprogrammed, if needed, from the satellite's umbilical port connection after final satellite assembly.

Although both processors meet our required attributes, we choose the PIC18LF6720. This is because PIC processors have been used on satellites in the past and there are more development environments and products for the PIC than for the Cygnal processors.

3.3.6 FLASH Memory Storage

An external storage device is needed to store payload data and satellite health information. The design for CP2 must incorporate an “adequate” amount of payload data storage. This presents a problem since the payload data storage requirements are unknown. The data storage requirement is instead determined by the rate of data download and the number of “ground station passes” required to downlink all of the payload data.

Our RF transceiver operates with a data transfer rate of 1200 bits per second. With an average of three ground station passes per day, an average pass time of 7 minutes, and a 40% protocol and packet loss overhead, this results in a rough daily downlink data rate of about 113kB. Ideally, the data storage device would be able to store several days worth of data. This would prevent CP2 from filling up its onboard memory and losing data if data could not be downlinked quickly enough.

As our data bus uses I^2C, we looked for I^2C mass memory devices. Most of the high storage capacity devices were FLASH based and have 64kB of memory. The devices often have an I^2C address bit selectable by tying a pin to Vcc or Ground. This feature allows two of the memory devices on the I^2C bus without any conflicts. With two 64kB devices, the total storage is 128kB or about one days worth of data storage.

Having more than one day worth of data storage would be preferable but not required. Fortunately, a 128kB FLASH I^2C memory device from Atmel was found. This device also has an external address pin which allows two devices on the same I^2C bus. By using theses devices, the total data storage on CP2 can be 256kB of memory, or the equivalent of over two days worth of data download. This quantity of data storage seems adequate for CP2 and a higher capacity I^2C memory device could not be found. The resulting data storage circuit is shown in Figure 33.

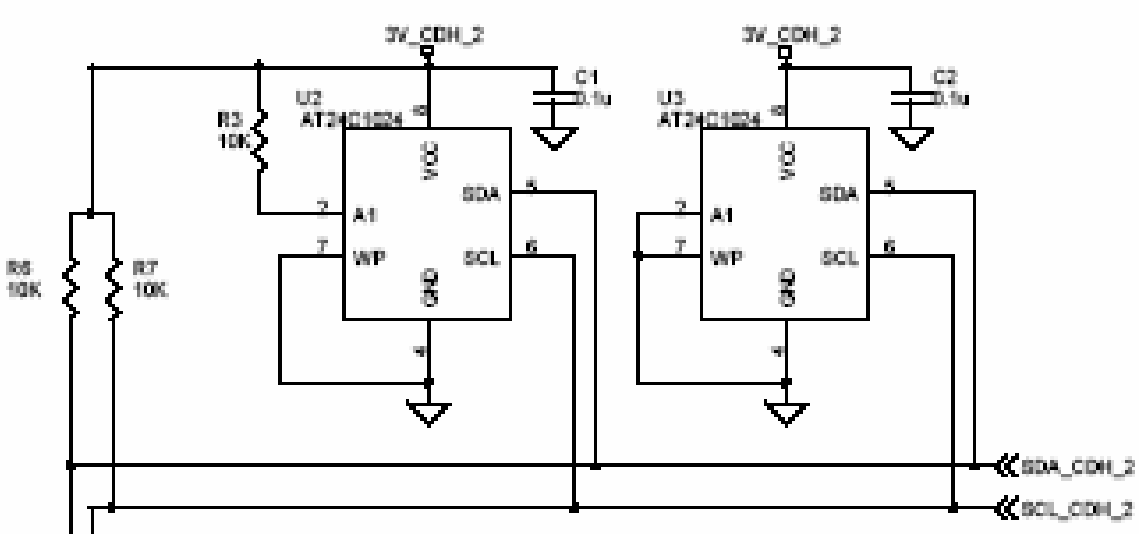

Figure 33. Memory storage circuit including two Atmel 24C1024 ICs storing 256kB of data in two 8-pin serial FLASH memory devices.

The circuit includes the two Atmel 24C1024 serial flash memory devices with associated bypass capacitors. This section of the I^2C bus also includes the main I^2C bus pull-up resistors.

By using serial FLASH memory devices and limiting the complexity of the memory storage circuit, this circuit is only 1.5 square centimeters of PCB real estate.

4 Design Modifications

4.1 C&DH Design Modifications

The design modifications on the C&DH system were minimal. Two types of modifications needed to be made. The first is that the analog low pass filter settings had

to be set by finding an appropriate Tau for noisy data acquisition signal lines. The other problem lied in a mysterious capacitance on the I^2C lines.

4.1.1 Low Pass Filter Setup

The low pass filter can be easily set by determining the settling time, the time interval between signal change and when the sample will be taken. For example, the peak power tracker requires solar panel voltage and current data. By software design, the time between solar panel voltage change and solar panel voltage and current data acquisition is 0.5 seconds. If we consider a Tau of one fifth of the settling time, Tau=0.1 seconds. With the 1uF capacitor installed by default into the side panels, the low pass filter resistor value comes to 100kΩ.

With this low pass filter installed, the reaction time of the data acquisition system may seem rather large but it is appropriate for the system.

Other low pass filters for CP2 do not have a precise settling time. Examples of this are the C&DH current or the SPA voltage low pass filters. For these cases, the noise seen on the analog line is monitored during satellite activity and an appropriate low pass filter is selected to remove the observed noise.

4.1.2 I^2C Capacitance Issue

A challenging problem occurred on the C&DH/Comm. Board I^2C lines. The I^2C lines to the right of the bridge in Figure 22 have an extreme capacitance well above the I^2C

specification. The initial I^2C data transfer curves are shown in Figure 34. The bus capacitance could not be traced to a single component or an incorrect board layout.

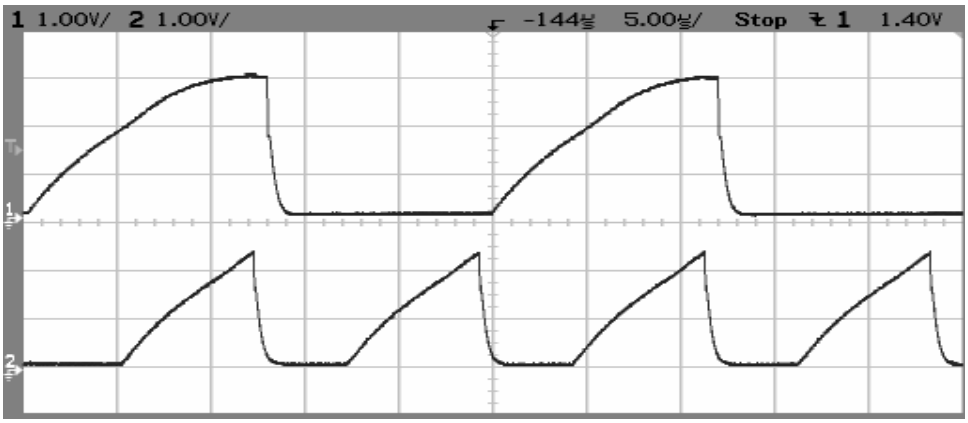

Figure 34. I^2C data on a highly capacitive bus.

One solution would be to use stronger pull-up resistors to create a much sharper rising edge on the waveform. While all devices on the I^2C bus can accept the lower resistance pull-up resistors, the I^2C multiplexer became a problem. It has a resistance of around 360Ω. With low resistance pull-up resistors, the resistance of the I^2C MUX prevents correct communication through the MUX. An example of the complications are shown in Figure 35 where the I^2C MUX resistance does not allow the data acquisition circuit to pull the I^2C data line (shown as input 2) below 1.8V.

Figure 35. I^2C data corrupted by devices unable to pull the data line below 1.8V.

The solution used was to insert an I^2C bus extender (P82B715TD) next to the I^2C bridge in Figure 36. The I^2C bus extender is used to attach a high-impedance I^2C bus to a low-impedance I^2C bus. By placing this device next to the bridge, the devices that can handle a low-impedance bus are isolated from the devices that can only work with a high-impedance bus but the two sides can still communicate with each other.

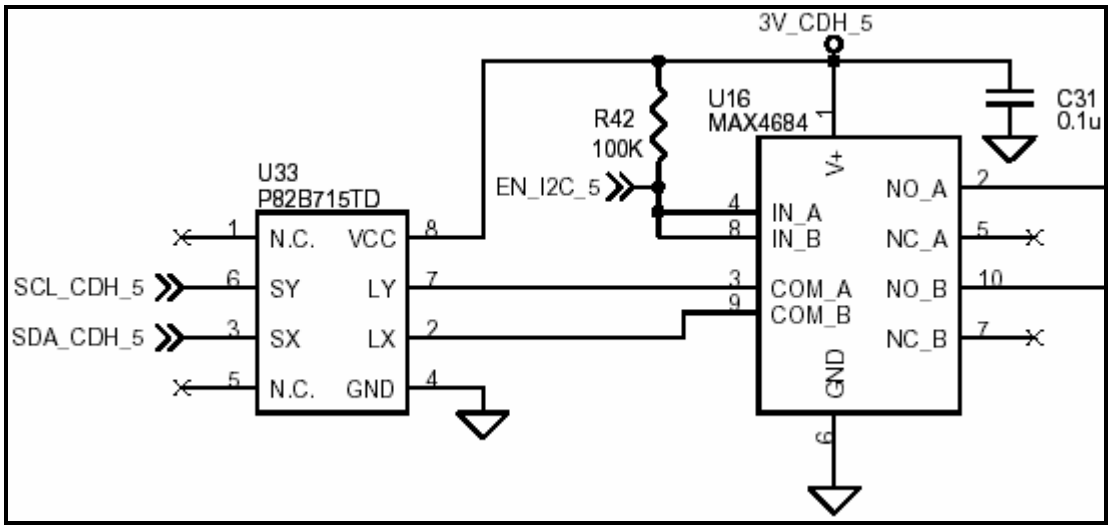

Figure 36. I^2C bridge with bus extender.

With this change implemented, the I^2C data waveform appears more square and all devices are able to pull the I^2C bus line to a logic low level. An I^2C transaction with the new circuit is shown in Figure 37.

Figure 37. I^2C data that can be correctly decoded by all I^2C devices.

Ideally, the I^2C data waveform should have a faster rise time. Further analysis should be done to determine the cause of this capacitance for capacitance reduction.

4.2 Electronic Power System Modifications

The power system modifications pertained to the PPT system and smart fuses on CP2. The smart fuses require resistor modifications to work properly and the PPT system required resistor changes and the addition of a component.

4.2.1 Smart Fuse Setup

The smart fuses need three resistor values set. The first resistor value sets the over-current threshold. The second resistor sets the delay before shut off and the third resistor determines the amount of time that the load is shut off for. These values must be set so that the load, when operating properly, does not trip the fuse. Also, the ratio between the time that the load is allowed to consume a high current and the time that the load is shut off should be minimized. The ratio should be such that the amount of power consume by a short circuit condition will not be detrimental to the power budget.

When power is first applied through the smart fuse, the smart fuse limits the load current to 1.5 times the over-current threshold. This current limiting means that a short period of time is required for the load voltage to reach its nominal value. While the voltage is ramping to the nominal value, the smart fuse considers the load to be in a fault condition. The amount of time that the smart fuse allows an over-current condition must be greater than the time required for the load voltage to reach its nominal value. An example of the C&DH system load branch power up is shown in Figure 38. If the smart fuse does not correctly apply power to the load, either the over-current threshold or the delay before shutoff must be modified to prevent the smart fuse from faulting during normal load activation.

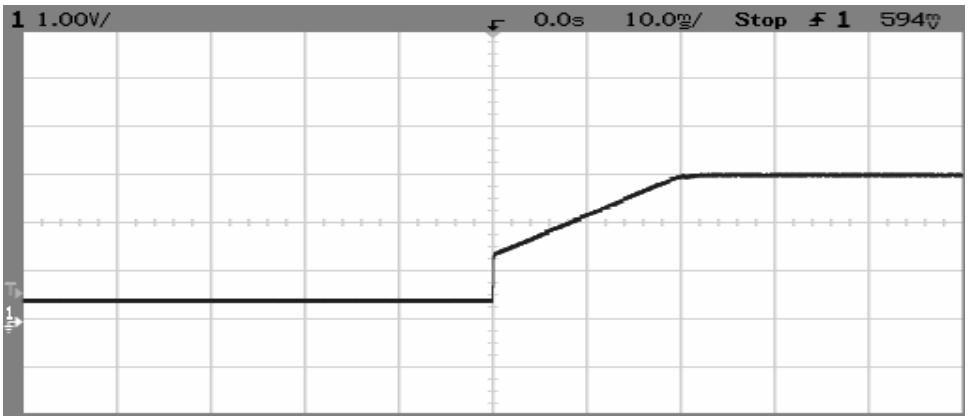

Figure 38. C&DH load branch voltage rising as the smart fuse turns on the load.

The time between retried can be determined by applying a low resistance across the load and observing the load voltage. Figure 39 shows the smart fuse trying and retrying to activate the load. In this case, the smart fuse waits three seconds before reapplying power to the load.

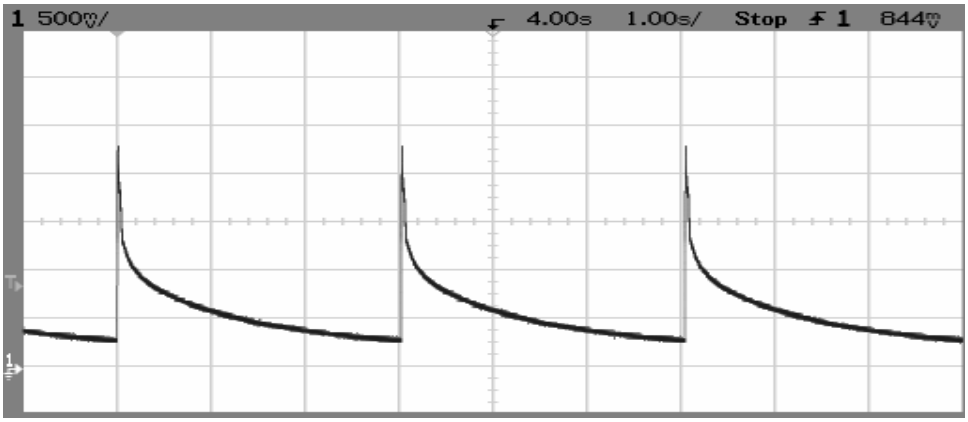

Figure 39. Load voltage as the smart fuse periodically retries to activate the load.

4.2.2 Peak Power Tracking Setup

Two difficulties in the peak power tracking system have been observed. One problem is that the system allows current to flow in reverse through solar panels and waste energy. Another problem is that the resistor values that set the solar panel set point voltage range need to be adjusted to appropriate values. Furthermore, the PPT system must be bypassed when its regulated 3V supply voltage is unavailable because it does not operate properly without the 3V supply voltage.

4.2.3 Ideal Diode Circuit

An ideal diode circuit allows current to flow out of the solar panel but prevents reverse current that allows the solar cells to consume power. The circuit in Figure 40 prevents reverse solar panel current by turning off a MOSFET whenever the solar panel voltage is less than the main bus voltage. It does this by measuring the voltage across the Drain and Source of the MOSFET to determine which direction current would flow if the MOSFET is turned on. If the current would flow in such a way that the solar panel will produce power, the MOSFET is turned on.

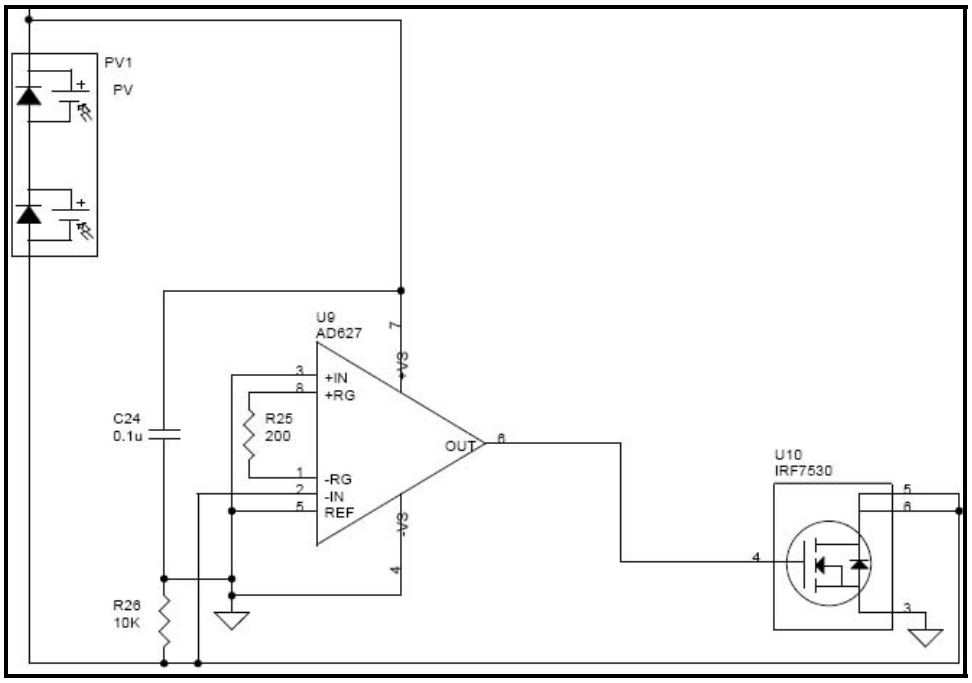

Figure 40. Solar Panel Ideal Diode Circuit.

This circuit is special in that it operates with either the solar panel power or the main bus power. The difference between these two power systems is the negative side connection. To allow the amplifier power from either the solar panels or the main bus, the negative terminal of the amplifier is attached to the main bus ground but is also attached to the solar panel ground through a 10k resistor. The amplifier consumes a small enough power that it can operate with a 10k resistor in series with it but the solar panel power lost through the 10k resistor is negligible.

4.2.4 Peak Power Tracker Bypass

A PPT bypass is needed to allow the solar panel power to reach the main power bus in the event that the PPT system is powered down and not operating. The solution can be very simple: All that is needed is to allow solar panel power to charge the batteries to a

minimal value until the 3V side panel power turns on. At that time the PPT can activate and allow current flow.

The solution chosen to allow solar panel current to flow when a battery is discharged is to bypass the PPT circuit with a silicon diode. The 0.7V to 0.8V drop of the diode will allow the solar panel voltage to charge the batteries to about 3.5V. At 3.4V the 3V power supplies to the side panels are enabled and the PPT turns on. By using a silicon diode, the voltage drop across the diode is large enough that it does not interfere with the PPT operation but can charge the batteries to a minimal charge state when needed.

4.2.5 Peak Power Tracking Resistor Values

The peak power tracking system requires two resistors to set the range of solar panel setpoint voltages. One resistor is in series above the digi-pot, and one resistor is in series below the digi-pot. These resistors set the percent of the solar panel voltage that the digi-pot can select from.

One difficulty with the peak power tracker is that the gate threshold voltage of the MOSFET in Figure 8 varies significantly with temperature. This requires that the values of the resistors around the digi-pot allow a wide range of resistor values used on CP2 have been selected to allow a large range of solar panel voltages. By selecting appropriate resistor values, the PPT system works properly over the full operating temperature range.

5 Future Work

Future work for this design mostly includes performance analysis of CP2. Analyses of the PPT system and battery circuits need to be done. The capacitance issue on the I^2C bus should be resolved.

The Peak Power Tracking system has not been analyzed for performance and the improvement over other solar charging methods should be done, for example. One challenge in doing this is the lack of an appropriate sun simulator to accurately simulate the spectrum of light incident on a satellite in low earth orbit. The analysis would have to use the CP2 model in a vacuum and an appropriate thermal shroud would be required in order to simulate the heat transfer environment.

The battery analysis would involve characterizing the battery voltage at various charge states, temperatures, and loads. This analysis would require a data acquisition system, power supply, electrical load, and a thermal chamber. The room temperature battery circuit testing for CP1 consumed about two months of time so a thorough battery circuit test for CP2 over the operating temperature range may take several months.

The capacitance on CP2's I^2C lines is mysteriously high and the source of the capacitance should be determined. While the I^2C bus works properly, it is outside of the official I^2C specification.

Future work may focus on advances on the circuit design. A better microcontroller may be chosen and integrated into CP2. If more data storage is required, a higher density memory storage circuit may be designed. If more energy storage is required, more batteries or higher energy density batteries may be used.

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List of Definitions

Attitude Control – Orientation and rotation control of a satellite.

C&DH – Command and Data Handling

DAQ – Data Acquisition System

Digi-pot – Digital Potentiometer

DOD- Depth of Discharge

EPS – Electronic Power System

I^2C – Inter–Integrated Circuit

MOSFET – Metal Oxide Semiconductor Field Effect Transistor

1-Wire Bus™ – A serial communications protocol.

P-POD – Poly Pico-satellite Orbital Deployer. A devices developed at Cal Poly University to deploy three CubeSats from a rocket.

RBF – Remove Before Flight. A pin used to disable a satellite before launch.

RS-232, RS-422, RS-485 – Various serial communications protocols.

SEL – Single Event Latchup. A radiation event that causes high current flow and can permanently damage electronic devices in space.

Appendix A

CP2 Final Schematic